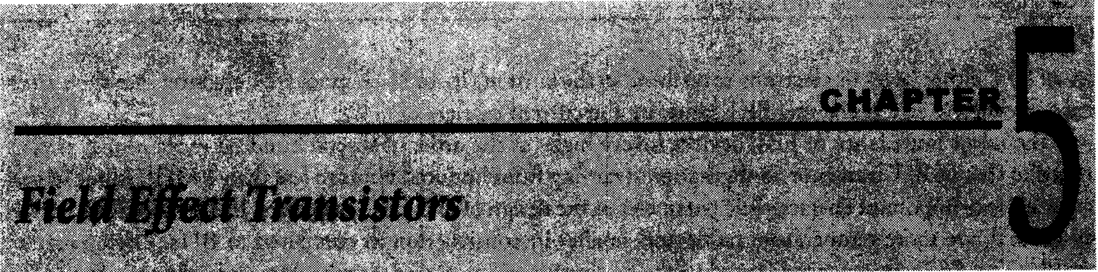


Learning Objectives

After completing this chapter, you will learn the following:

- Comparison between FETs and BJTs.
- Types of FETs: JFETs and MOSFETs.
- Construction and operation of JFETs.
- Construction and operation of MOSFETs.
- Comparison between JFETs and MOSFETs.
- FET biasing configurations: common-gate, common-source (fixed-bias, self-bias, voltage-divider-bias and feedback-bias configurations) and common-drain configurations.
- Handling and testing of FET devices.
- Introduction to VMOS, CMOS and IGBT devices.

Field effect transistors (FETs) are three-terminal semiconductor devices where the conduction path is controlled by an electric field established by the carriers present in the device. The concept of FETs predates that of bipolar junction transistors (BJTs) but they were physically implemented after BJTs due to limitations of semiconductor technology. FETs can be classified into two types, namely, the junction FETs (JFET) and metal-oxide-semiconductor FETs (MOSFET) depending upon their construction and mode of operation. MOSFETs are further classified as enhancement MOSFETs and depletion MOSFETs. The focus in this chapter is FETs. The topics covered include comparison between FETs and BJTs, construction and operation of JFETs and MOSFETs, followed by commonly used biasing circuits for both types of devices. Testing and handling FET devices is also covered in the chapter. The chapter concludes with a brief description of vertical MOS (VMOS), complementary MOS (CMOS) and insulated gate bipolar transistors (IGBT).

5.1 Bipolar Junction Transistors versus Field Effect Transistors

Both BJTs and FETs are semiconductor devices. The major difference between the two devices is that BJTs are current-controlled devices whereas FETs are voltage-controlled devices. In a BJT, the collector current (I_C) is a direct function of the base current (I_B) whereas in an FET, the drain current (I_D) depends upon the gate-source voltage (V_{GS}). In other words, in a BJT the output current is controlled by the input current whereas in an FET it is controlled by the input voltage.

Another important difference between the two devices is that BJTs are bipolar devices whereas FETs are unipolar devices. In other words, in a BJT both electrons and holes contribute to the flow of current whereas

in an FET either holes or electrons contribute to the current. In an N-channel FET electrons are the current carriers whereas in a p-channel FET holes are the current carriers.

The input impedance of FET devices is very high (of the order of several hundred mega-ohms) as compared to that of BJT transistor configurations (varying from hundred ohms to less than 1 MΩ). Input impedance is a very important characteristic parameter in the design of linear AC amplifiers. In addition, FET devices, in general, are more temperature stable and smaller in construction as compared to BJTs. Owing to their smaller size, FETs are extensively used in the fabrication of integrated circuits. However, the gain of an FET-based amplifier is smaller as compared to a BJT amplifier, that is, FET amplifiers have poorer sensitivity to changes in the input signal. Also FETs are more sensitive to handling than BJTs.

5.2 Junction Field Effect Transistors

Junction FET (JFET) is the simplest of the FETs. It is a three-terminal device where the voltage applied at one terminal controls the current through the other two terminals. JFETs comprise a semiconductor channel embedded into semiconductor layers of opposite polarity. Depending upon whether the semiconductor channel is an N-type semiconductor or a P-type semiconductor, JFETs are classified as N-channel or P-channel JFETs, respectively.

Construction and Principle of Operation

Figures 5.1(a) and (b) show the cross-sectional view of N-channel and P-channel JFETs, respectively. As we can see from the figures, in an N-channel JFET, an N-type semiconductor material forms a channel between embedded layers of P-type material whereas in a P-channel JFET, a P-type semiconductor forms a channel between the embedded layers of N-type material. Therefore, two P–N junctions are formed between the semiconductor channel and the embedded semiconductor layers. Ohmic contacts are made at the top and bottom of the channel and are referred to as the drain (D) and the source (S) terminals, respectively. The channel behaves as a resistive element between its drain and source terminals. In an N-channel JFET, both the embedded P-type layers are connected together and form the gate (G) terminal. Similarly in a P-channel JFET, the gate terminal is formed by connecting the two N-type embedded layers. Figures 5.2(a) and (b) show the circuit symbols for the N-channel and P-channel JFETs, respectively.

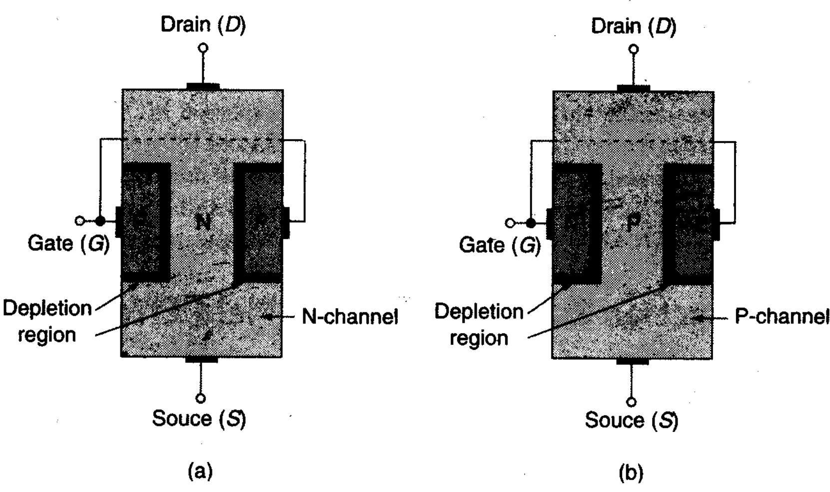


Figure 5.1 | Cross-section of (a) an N-channel JFET; (b) a P-channel JFET.

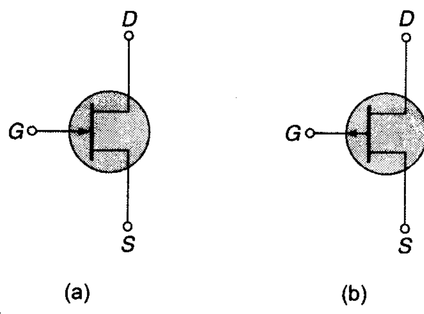


Figure 5.2 | Circuit symbol of (a) an N-channel JFET; (b) a P-channel JFET.

In the absence of any externally applied potential, both the P–N junctions are open circuit and a small depletion region is formed at each of the junctions as shown in Figure 5.1. The externally applied potential between gate and source terminals controls the flow of drain current for a given potential between the drain and source terminals. The operation of JFET devices is explained in the subsequent sections.

Characteristic Curves

In this section, the principle of operation of an N-channel JFET is explained. The operation of a P-channel JFET is similar to that of an N-channel JFET with the polarities of voltages and direction of currents reversed. Let us consider the situation when a positive drain-source voltage (V_{DS}) is applied to the JFET with gate terminal shorted to the source terminal ($V_{GS} = 0$).

Figure 5.3(a) shows the circuit connection. When the drain-source voltage is applied, the electrons in the N-channel are attracted to the drain-terminal establishing the flow of drain current (I_D) as shown in Figure 5.3(b). The value of I_D is determined by the value of the applied V_{DS} and the resistance of the N-channel between the drain and the source terminals. Owing to the flow of I_D, there is a uniform voltage drop across the

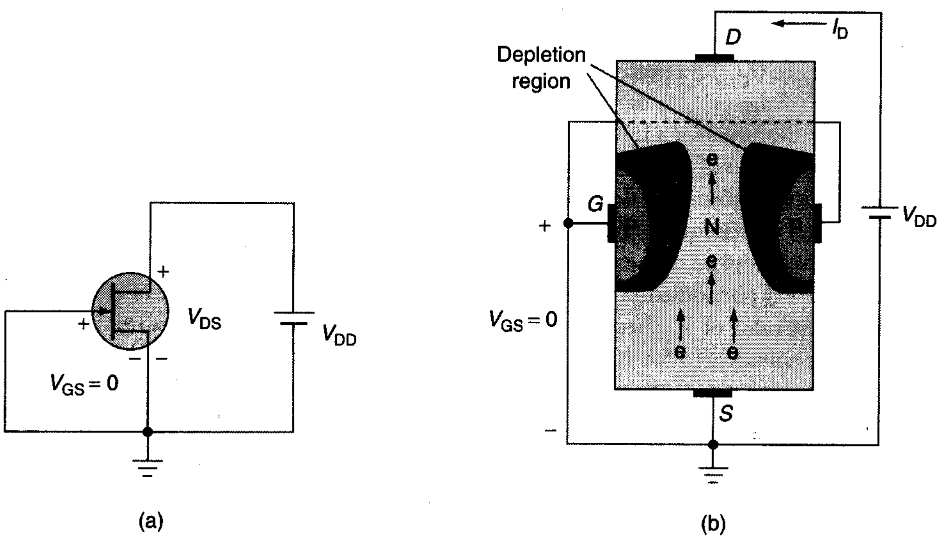


Figure 5.3 | N-channel JFET with V_{GS} = 0 and positive value of V_{DS}.

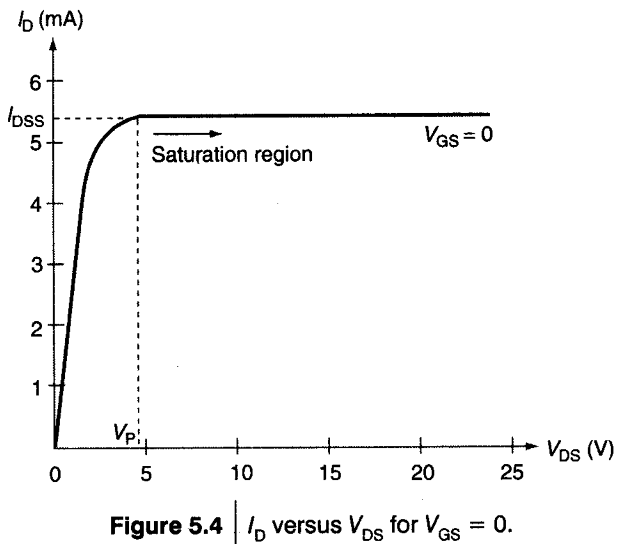


Figure 5.4 I_D versus V_{DS} for $V_{GS} = 0$.

channel resistance, which reverse biases the two P–N junctions. This results in increase in the width of the depletion region. It may be mentioned here that the depletion region is wider near the drain-region than the source-region. This is because I_D and the channel resistance establish more reverse-bias voltage at the P–N junction near the drain-region than near the source-region.

I_D increases linearly with increase in V_{DS} till the V_{DS} reaches a value where the saturation effect sets in. This is evident from Figure 5.4 which shows the relationship between I_D and V_{DS} for zero V_{GS} ($V_{GS} = 0$). The value of V_{DS} where the saturation effect sets in is referred to as the pinch-off voltage (V_P). When V_{DS} reaches V_P, the value of I_D does not change with further increase in the value of V_{DS}. This condition is referred to as the pinch-off condition. This happens because the width of the depletion regions of the P–N junctions has increased significantly near the drain-region resulting in reduction of the channel width (Figure 5.5). Therefore, I_D essentially remains constant for $V_{DS} > V_P$. This current is referred to as the drain-to-source current for short circuit connection between gate and source (I_{DSS}). In nutshell, for $V_{DS} > V_P$, JFET has characteristics of a constant current source.

The gate-source voltage (V_{GS}) is the control voltage for JFETs in the same way as the base current (I_B) is for BJTs. The characteristic curves for a JFET are plotted between the drain current (I_D) and the drain-source voltage (V_{DS}) for different values of V_{GS}. In case of an N-channel JFET, the voltage V_{GS} is negative, that is, the gate terminal is made more negative than the source terminal. Voltage V_{GS} is positive for P-channel JFETs.

Figure 5.6 shows the circuit connection when both drain and gate voltages are applied to the JFET. When a negative bias is applied to the gate terminal, there is an increase in the width of the depletion region. Therefore, the pinch-off phenomenon occurs at lower values of V_{DS}. Also, the value of saturation drain current decreases. As the value of V_{GS} becomes more negative the value of saturation current decreases further. The drain current becomes zero for V_{GS} equal to $-V_P$. This voltage is referred to as the gate-source cut-off voltage or the gate-source pinch-off voltage ($V_{GS(off)}$).

In fact, the value of drain-source pinch-off voltages decreases in a parabolic manner with the V_{GS} becoming more negative. Figure 5.7 shows the output characteristic curves for the N-channel JFET. The region to the left of the locus of pinch-off voltages is the Ohmic region or the voltage-controlled resistance region. Region to the right of the locus of the pinch-off voltages is the saturation region or the constant-current region. In the Ohmic region, JFET acts as a variable resistor whose resistance is controlled by the applied gate-source voltage.

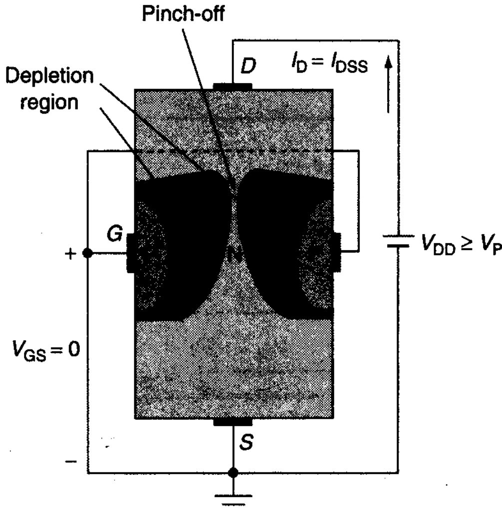


Figure 5.5 | N-channel JFET with $V_{GS} = 0$ and $V_{DS} \geq V_P$.

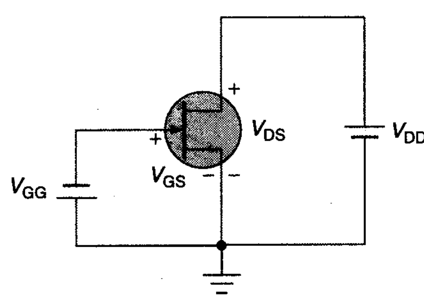


Figure 5.6 | N-channel JFET biasing circuit.

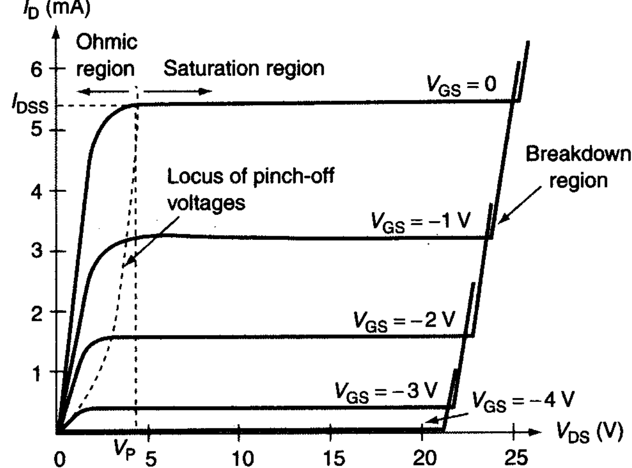


Figure 5.7 | Output characteristic curves of an N-channel JFET.

The drain resistance (r_d) in the saturation region is given by Eq. (5.1)

$$r_d = \frac{r_o}{(1 - V_{GS}/V_p)^2} \tag{5.1}$$

where r_o is the resistance at $V_{GS} = 0$; r_d is the resistance at a particular value of V_{GS}; V_P is the pinch-off voltage.

The relationship between the output current I_D in the saturation region for a given value of input V_{GS} is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \tag{5.2}$$

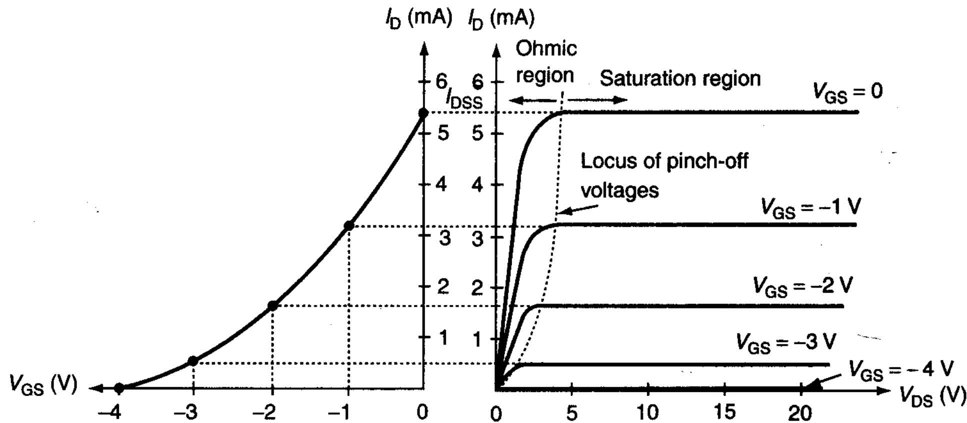


Figure 5.8 | Transfer characteristic curves of N-channel JFET.

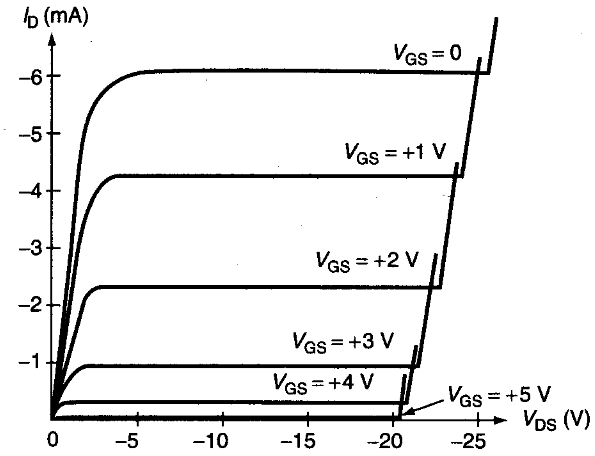


Figure 5.9 | Characteristic curve of P-channel JFET.

where I_{DSS} is the drain current for short circuit connection between gate and source. This expression is referred to as the Shockley's equation. As is clear from the equation there is a non-linear square law relationship between the output drain current (I_D) and the input gate-source voltage (V_{GS}) as opposed to a linear relation between the output collector current (I_C) and the input base current (I_B) in case of BJTs. Because of the square law characteristics, JFETs are very useful devices in radio tuners and TV receivers.

The transfer characteristics of an FET device is a plot between I_D and V_{GS} and can be plotted using Shockley's equation or using the output characteristic curves. Figure 5.8 shows how we can obtain the transfer characteristics curves using the output characteristics curves.

As mentioned before, P-channel JFETs behave in the same manner as the N-channel JFETs with the direction of currents and polarities of voltages reversed. Figure 5.9 shows the output characteristic curves for P-channel JFETs.

Effect of Temperature on JFET Parameters

JFETs offer better thermal stability as compared to BJTs. Increase in JFET temperature results in decrease in the depletion region width and decrease in the carrier mobility. Decrease in the width of depletion region

results in increase in channel width, which in turn increases in I_D. This results in positive temperature coefficient for I_D. Increase in I_D with temperature results in increase in $V_{GS(off)}$ with temperature. $V_{GS(off)}$ also has a positive temperature coefficient of the order of 2.2 mV/°C.

Decrease in carrier mobility gives I_D a negative temperature coefficient. Since both the mechanisms occur simultaneously, the effect of one mechanism compensates for the other. Therefore, JFETs offer better temperature stability. It is even possible to bias the JFET so as to establish zero temperature coefficient.

5.3 Metal Oxide Field Effect Transistors

Metal oxide FET (MOSFET) is insulated from the semiconductor channel by a very thin oxide layer. MOSFETs are also referred to as insulated gate field effect transistors (IGFETs). Like a JFET, a MOSFET is also a three-terminal device where the drain current is controlled by the applied gate voltage.

MOSFETs are further classified into two types depending upon their construction and mode of operation, namely, the depletion MOSFET (or DE-MOSFET) and the enhancement MOSFET (or E-MOSFET). In this section, we discuss the construction, principle of operation and characteristic parameters of both the types of MOSFETs. Also discussed are the precautions to be taken while handling MOSFETs.

Depletion MOSFETs

In a DE-MOSFET, a channel is physically constructed between the drain and the source terminals. DE-MOSFETs are further classified as N-channel DE-MOSFETs and P-channel DE-MOSFETs depending on whether the channel material is an N-type semiconductor or a P-type semiconductor.

The cross-sectional view of an N-channel DE-MOSFET is shown in Figure 5.10. It comprises a substrate made of a P-type semiconductor material. Two N+ type regions linked by an N-channel are formed on the substrate. The source and the drain terminals are formed by connecting metal contacts to the two N+ regions as shown in Figure 5.10. The gate terminal is connected to the insulating silicon dioxide (SiO_2) layer on top of the N-channel. Therefore, there is no direct electrical connection between the gate terminal and the channel of a DE-MOSFET. (In case of E-MOSFETs also, there is no direct electrical connection between the gate terminal and the channel.) There is a capacitance that exists between the gate and the channel as the metal gate contact and the channel act as walls of a parallel plate capacitor and the SiO_2 layer forms the dielectric. Hence the input impedance of a DE-MOSFET is very high of the order of 10^{10}–10^{15} Ω.

The construction of a P-channel DE-MOSFET (Figure 5.11) is similar to that of an N-channel DE-MOSFET with the difference being that the substrate is an N-type semiconductor while the channel is a P-type material. Figures 5.12(a) and (b) show the circuit symbols for N-channel and P-channel DE-MOSFETs, respectively.

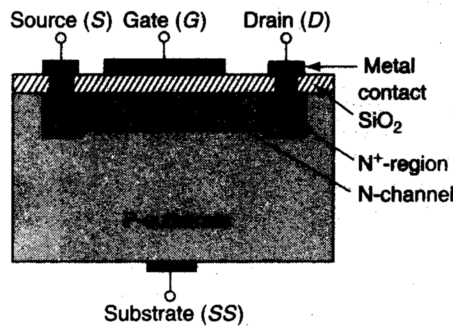


Figure 5.10 Cross-section of an N-channel DE-MOSFET.

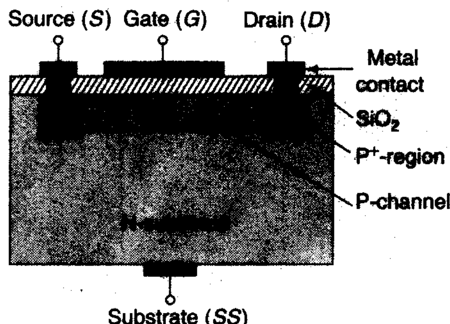


Figure 5.11 Cross-section of a P-channel DE-MOSFET.

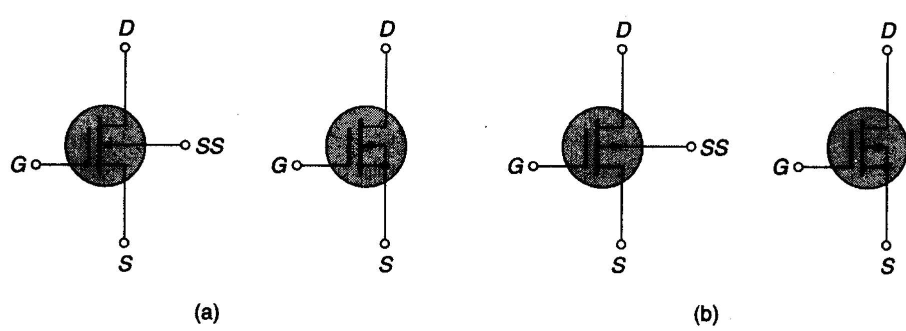


Figure 5.12 Circuit symbol of (a) an N-channel DE-MOSFET; (b) a P-channel DE-MOSFET.

Let us now see how the N-channel DE-MOSFET operates. When the gate and the source terminals are shorted, that is, the voltage $V_{GS} = 0$ and a positive voltage is applied between the drain and the source terminals, that is, voltage V_{DS} is positive (Figure 5.13), there is a flow of current in the N-channel as the electrons are attracted by positive potential at the drain terminal. The current increases with increase in V_{DS} and after a certain value of V_{DS} it becomes constant. This current is represented as I_{DSS} and is similar to that established in a JFET with $V_{GS} = 0$. When the gate terminal is at a negative potential as compared to the source terminal, electrons in the N-channel are repelled by this negative potential towards the P-type substrate. Also, the holes in the P-type substrate are attracted towards the gate. This results in recombination of holes and electrons and there is reduction in the number of free electrons in the N-channel (Figure 5.14). The higher the negative potential, more is the rate of recombination and less the number of free electrons in the channel. Therefore the drain current decreases with increase in the value of the negative gate-source potential.

For positive values of gate-source voltage, electrons (minority carriers) in the P-type substrate are attracted into the channel and establish new carriers through the collisions between accelerating particles. Thus the drain current increases rapidly with increase in the positive value of gate-source voltage. As the application of positive gate-source voltage increases the value of drain current, the region of positive gate-source voltages is referred to as the enhancement region. The region for zero and negative values of gate-source voltage is referred to as the depletion region. It may be mentioned here that Shockley's equation as defined for JFETs is applicable for DE-MOSFETs also in both the depletion and the enhancement regions. Figure 5.15 shows the output characteristic curves for an N-channel DE-MOSFET.

The transfer characteristics for DE-MOSFET can be plotted in a similar fashion for that of a JFET. Figure 5.16 shows the transfer characteristics for an N-channel DE-MOSFET.

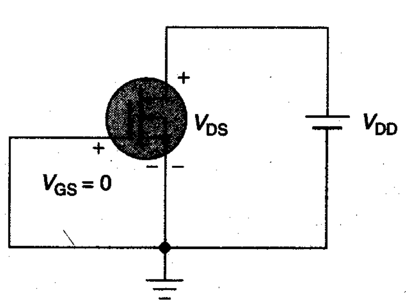


Figure 5.13 Circuit connection of N-channel DE-MOSFET.

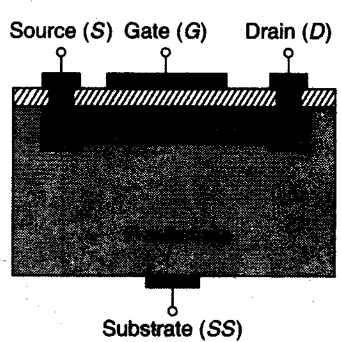


Figure 5.14 N-channel DE-MOSFET.

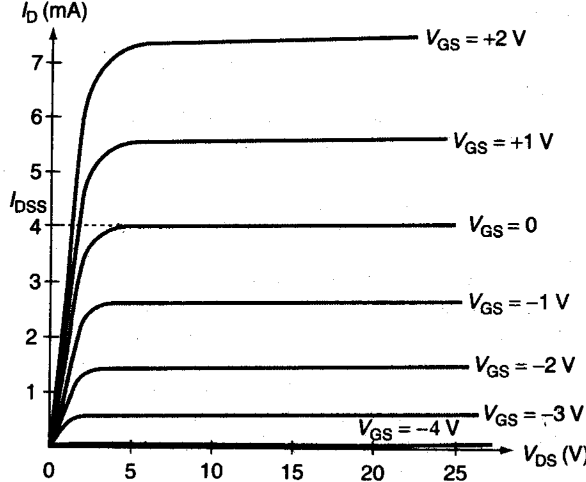


Figure 5.15 | Output characteristic curves of N-channel DE-MOSFET.

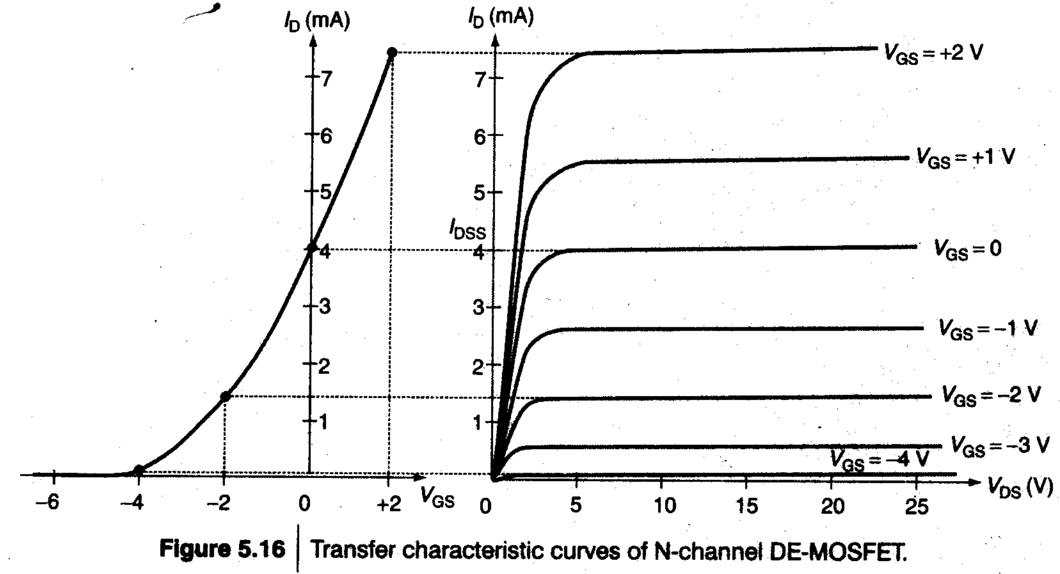


Figure 5.16 | Transfer characteristic curves of N-channel DE-MOSFET.

Enhancement MOSFETs

The construction of an E-MOSFET is similar to that of a DE-MOSFET with the difference that there is no physical channel between the source and drain terminals in the E-MOSFET. The invention of E-MOSFETs has revolutionized the computer industry and they are extensively used in digital electronics and computers. Figures 5.17(a) and (b) show the cross-section of N-channel and P-channel E-MOSFETs, respectively. Figures 5.18(a) and (b) show the circuit symbols of the N-channel and P-channel MOSFETs, respectively. The broken line in the symbol indicates the absence of a channel.

The N-channel E-MOSFET functions as follows. When the gate-source voltage is zero and some positive drain-source voltage is applied there is no drain current as there is no channel available for flow of drain current. E-MOSFETs are also normally called OFF MOSFETs as they do not conduct when $V_{GS} = 0$. The drain current flows only when a positive voltage is applied to the gate terminal with respect to the source terminal as this induces

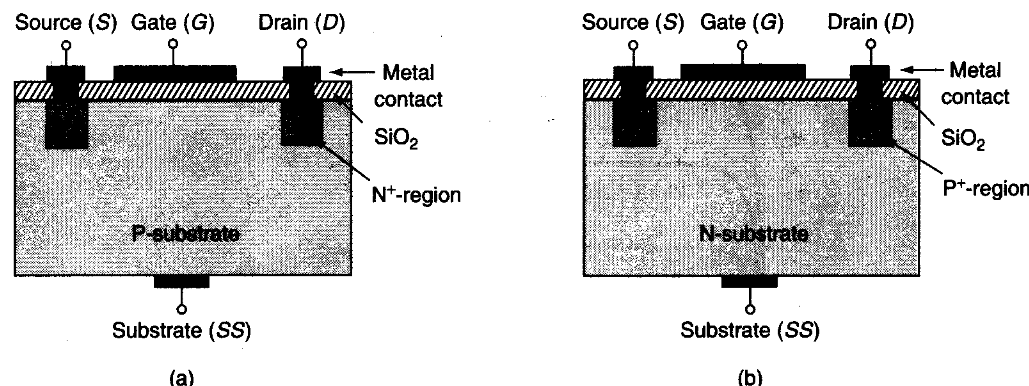


Figure 5.17 (a) Cross-section of an N-channel E-MOSFET; (b) cross-section of a P-channel E-MOSFET.

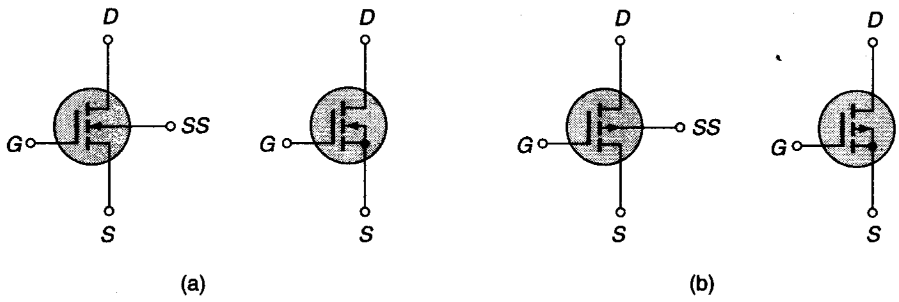


Figure 5.18 Circuit symbol of an N-channel E-MOSFET; (b) circuit symbol of a P-channel E-MOSFET.

a channel by drawing the electrons (minority carriers) in the P-type substrate to accumulate near the surface of the SiO_2 layer. Also, holes in the P-substrate are forced to move away from the edge of the SiO_2 layer as shown in Figure 5.19. As the SiO_2 layer is insulating, it prevents the electrons from being absorbed at the gate terminal. These electrons lead to the flow of current between the drain and the source terminals. As the value of gate-source voltage is increased, more and more electrons accumulate leading to an enhanced flow of drain current. The level of gate-source voltage that leads to significant flow of drain current is referred to as threshold voltage and is denoted by V_T. For a fixed gate-source voltage and increasing the level of drain-source voltage leads to an initial increase in the drain current which eventually saturates due to the reduction in the gate-drain voltage (V_{GD}) with increase in the drain-source voltage (V_{DS}). Reduction in the gate-drain voltage reduces the attractive forces for the free carriers in the induced channel near the drain region, resulting in the reduction of effective channel width near the drain region. This effect is referred to as the pinching effect. Pinching effect refers to the reduction in the width of the channel near the drain region with increase in the drain-source voltage (Figure 5.20). The value of the drain-source voltage at which the drain current saturates is given by $V_{DS(sat)}$.

Figure 5.21 shows the output characteristic curves for an n-channel E-MOSFET. It can be observed from the curve that the $V_{DS(sat)}$ voltage increases with the increase in the applied gate-source voltage. The relationship between $V_{DS(sat)}$ and V_{GS} is given by

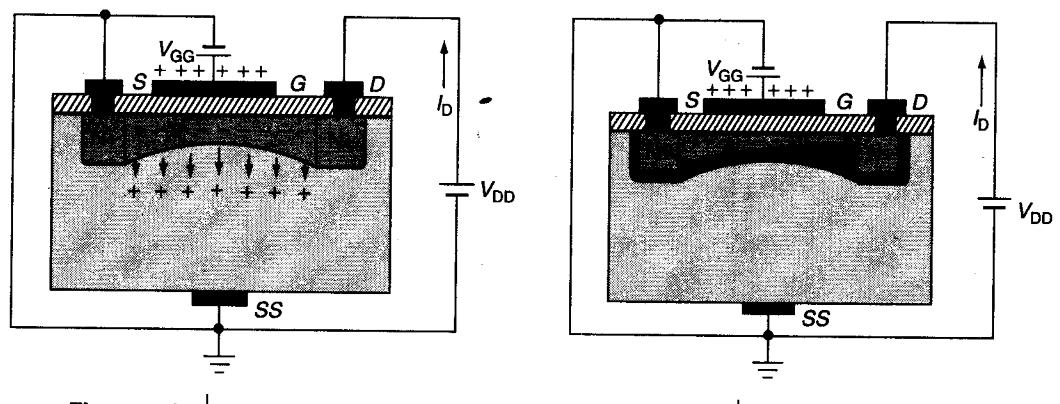


Figure 5.19 Working of N-channel E-MOSFET.

Figure 5.20 Pinching phenomenon in E-MOSFET.

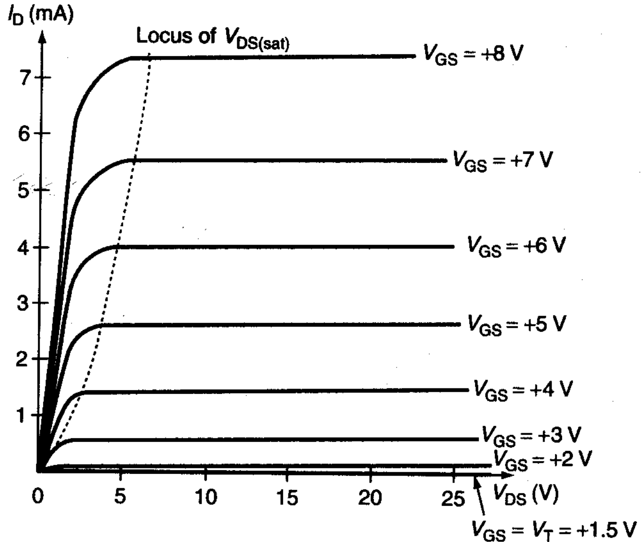


Figure 5.21 Output characteristic curves for an N-channel E-MOSFET.

$$V_{DS(sat)} = V_{GS} - V_T \tag{5.3}$$

where V_T is the threshold gate-source voltage.

Also, the drain current is zero for gate-source voltage less than the threshold voltage V_T. For voltages greater than the threshold voltage the drain current is given by

$$I_D = K(V_{GS} - V_T)^2 \tag{5.4}$$

where K is a constant. As is clear from Eq. (5.4), the relationship between the drain current and the gate-source voltage is non-linear and the current is proportional to the square of the voltage. The relationship is shown in Figure 5.22. The characteristics of Figure 5.22 are referred to as the transfer characteristics.

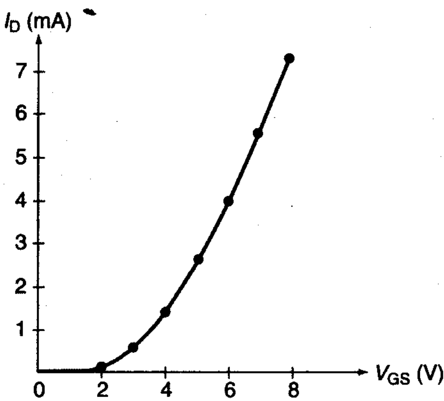


Figure 5.22 | Transfer characteristics of an N-channel E-MOSFET.

EXAMPLE 5.1

Identify the MOSFET shown in Figure 5.23. Given that V_T is the threshold voltage of the MOSFET, I_{DS} is the drain current of the MOSFET when the gate-source voltage is equal to twice the threshold voltage, draw its output characteristics. An external supply V_{GG} is applied between the gate and the drain terminals. Draw the curve between the drain current and voltage V_D for $V_{GG} = V_T/2$.

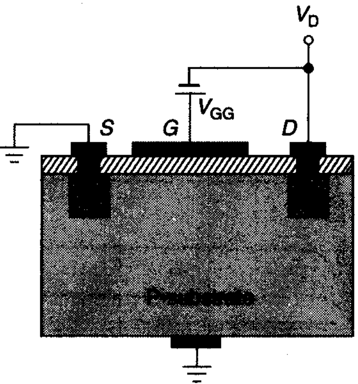


Figure 5.23 | Example 5.1.

Solution

1. The MOSFET shown in the figure is an N-channel E-MOSFET. As we have studied, E-MOSFET conducts for V_{GS} greater than the threshold voltage (V_T). The current in an E-MOSFET is given by $I_D = K(V_{GS} - V_T)^2$. As I_{DS} is the current for $V_{GS} = 2V_T$, therefore $K = I_{DS}/V_T^2$.
2. The output characteristics can be plotted using the equations

$$I_D = \frac{I_{DS}}{V_T^2}(V_{GS} - V_T)^2$$

$$V_{DS(sat)} = V_{GS} - V_T$$

As an example consider $V_{GS} = 3.5V_T$, $I_D = 6.25I_{DS}$ and $V_{DS(sat)} = 2.5V_T$. By calculating the values of I_D for different values of V_{GS} we can plot the output characteristic curves for the given MOSFET. Figure 5.24 shows the output characteristics of the given E-MOSFET.

3. The voltage V_{GG} is applied between the gate and the drain terminals. The gate-source voltage (V_{GS}) is given by $V_{GS} = V_{GG} + V_{DS} = V_{GG} + V_D$. (The voltage V_D is equal to the drain-source voltage V_{DS}.)
4. As $V_{GG} = V_T/2$, the voltage V_{GS} will be less than the threshold voltage V_T until voltage V_{DS} is less than $V_T/2$. When $V_D = V_T/2$, $V_{GS} = V_T$ and the MOSFET starts conducting after that.
5. Table 5.1 lists the values of V_{GS}, I_D for various values of V_D.
6. Figure 5.25 shows the plot of points corresponding to Table 5.1. The curve obtained by joining the points is the I_D versus V_D plot for $V_{GG} = V_T/2$.

Table 5.1 | Solution to Example 5.1

V_D	V_{DS}	V_{GS}	I_D
0	0	$0.5V_T$	0
$0.5V_T$	$0.5V_T$	V_T	0
V_T	V_T	$1.5V_T$	$0.25I_{DS}$
$1.5V_T$	$1.5V_T$	$2V_T$	I_{DS}
$2V_T$	$2V_T$	$2.5V_T$	$2.25I_{DS}$
$2.5V_T$	$2.5V_T$	$3V_T$	$4I_{DS}$
$3V_T$	$3V_T$	$3.5V_T$	$6.25I_{DS}$

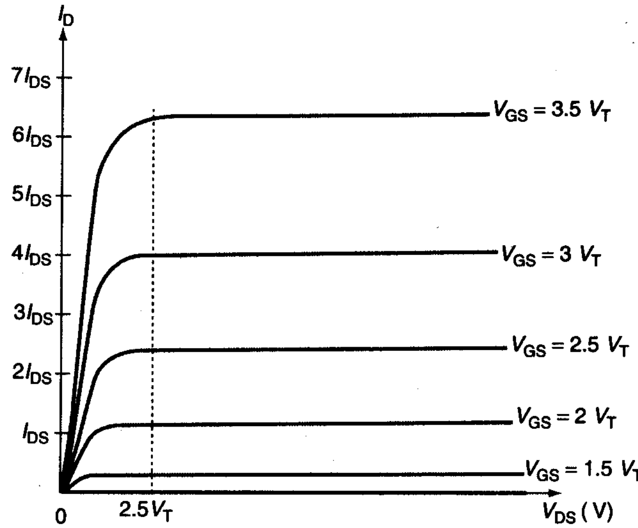


Figure 5.24 | Solution to Example 5.1.

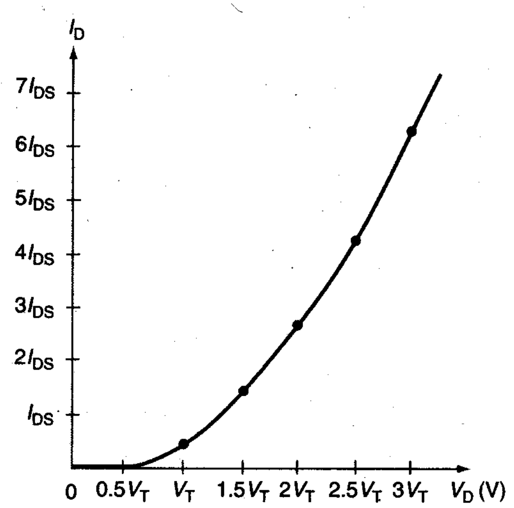


Figure 5.25 | Solution to Example 5.1.

Answer: Figure 5.24 shows the output characteristics and Figure 5.25 shows the I_D versus V_D plot.

5.4 FET Parameters and Specifications

In this section we describe the characteristic parameters and specifications of FETs.

Characteristic Parameters

Parameters used to define the performance of an FET device are static and dynamic drain resistance, transconductance (g_m) and amplification factor (μ).

Drain Resistance

Static drain resistance (R_D) is defined as the ratio of the drain-source voltage (V_{DS}) to the drain current (I_D):

$$R_D = \frac{V_{DS}}{I_D} \tag{5.5}$$

Dynamic drain resistance (r_d) is defined as the ratio of change in the drain-source voltage to the change in the drain current at a constant gate-source voltage.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{const.}} \tag{5.6}$$

The typical values of r_d lie in the range of 0.1 to 1 MΩ for JFETs and and in the range of 1 to 50 kΩ for MOSFETs.

Transconductance (g_m)

Transconductance (g_m) is defined as the ratio of the change in the drain current to the change in the gate-source voltage for a constant drain-source voltage:

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} = \text{const.}} \tag{5.7}$$

The transconductance varies with the applied-gate source voltage (V_{GS}) as given in Eq. (5.8):

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) \tag{5.8}$$

where g_{m0} is the transconductance at zero gate-source voltage. The value of g_m is in the range of 0.1 to 10 mA/V for JFETs and between 0.1 and 20 mA/V or more for MOSFETs.

Amplification Factor (μ)

Amplification factor (μ) is defined as the ratio of the change in the drain-source voltage to the change in the gate-source voltage for a constant value of drain current:

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D = \text{const.}} \tag{5.9}$$

Substituting the value of r_d given in Eq. (5.6) and the value of g_m given in Eq. (5.7) in Eq. (5.9) we get

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d \times g_m \tag{5.10}$$

Therefore, the amplification factor is the product of the dynamic drain resistance and the transconductance of the FET. Amplification factor in a JFET can be as high as 100.

EXAMPLE 5.2 *A given JFET device has a drain current of 8 mA when a drain voltage of 5 V is applied to it with gate-source terminals shorted. When the drain voltage is increased to 10 V there is a small increase in the drain current and the new value of drain current is 8.2 mA. When the gate-source voltage is made −0.4 V, the drain current decreases to 7 mA. Determine the type of the JFET, its drain resistance, transconductance and amplification factor.*

Solution

1. Since application of negative gate-source voltage results in decrease of the drain current, the JFET is an N-channel JFET.
2. Drain resistance

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} = \text{const.}}$$

$$r_d = (10 - 5)/(8.2 \times 10^{-3} - 8.0 \times 10^{-3}) = 5/(0.2 \times 10^{-3}) = 25\ \text{k}\Omega.$$

3. Transconductance

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} = \text{const.}}$$

$$g_m = (7\times10^{-3} - 8.2\times10^{-3})/(-0.4-0) = -1.2\times10^{-3}/(-0.4) = 3\ \text{mA/V}$$

4. Amplification factor

$$\mu = r_d \times g_m$$
$$= (25\times10^3)\times(3\times10^{-3}) = 75$$

Answer: JFET is an N-channel JFET, drain resistance = 25 kΩ, transconductance = 3 mA/V and amplification factor = 75.

EXAMPLE 5.3 *Derive the expression for the transconductance (g_m) of a JFET.*

Solution

1. The equation for the drain current (I_D) in a JFET is given by

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

2. Differentiating both the sides of the equation w.r.t. the gate-source voltage (V_{GS}) we get

$$\frac{dI_D}{dV_{GS}} = 2I_{DSS}\times\left(1-\frac{V_{GS}}{V_P}\right)\times\left(\frac{-1}{V_P}\right)$$

3. As $g_m = dI_D/dV_{GS}$. Therefore,

$$g_m = 2I_{DSS}\times\left(1-\frac{V_{GS}}{V_P}\right)\times\left(\frac{-1}{V_P}\right)$$

4. Let g_{m0} be the transconductance for $V_{GS} = 0$. Therefore,

$$g_{m0} = 2I_{DSS}\times\left(\frac{-1}{V_P}\right)$$

5. Substituting the value of g_{m0} in the expression for g_m we get

$$g_m = g_{m0}\times\left(1-\frac{V_{GS}}{V_P}\right)$$

Answer: The expression for transconductance of a JFET is given by

$$g_m = g_{m0}\times\left(1-\frac{V_{GS}}{V_P}\right)$$

FET Datasheet Specifications

An FET datasheet provides similar information as a BJT datasheet such as the device's maximum ratings, mechanical data and electrical characteristics. The common electrical specifications mentioned in datasheets of JFET and MOSFET devices are as follows:

1. **Reverse Gate-Source Breakdown Voltage (BV_{GS}):** It is defined as the reverse gate-source voltage with either the drain open (BV_{GSO}) or drain shorted to the source (BV_{GSS}). It is typically few tens of volts.
2. **Power Dissipation (P_D):** Power dissipation rating of the JFET is the product of the drain-source voltage (V_{DS}) and the drain current (I_D). The power dissipation rating must be derated with increase

in temperature. It is usually specified at an ambient of 25°C. JFETs are available in power ratings of hundreds of milliwatts while MOSFETs are available in a wide range of power ratings starting from a few milliwatts to more than hundred watts.

3. **Saturation Drain Current (I_{DSS}):** It is the maximum drain current when the gate terminal is shorted to the source terminal. It is usually specified at a given drain-source voltage somewhere in the channel pinch-off region.
4. **Pinch-Off Voltage (V_P or $V_{GS(off)}$):** It is the gate-source voltage for which the drain current reduces to zero. It is also specified for a given value of drain-source voltage. It is specified in case of JFETs and DE-MOSFETs only.
5. **Gate Leakage current (I_{GSS}):** It is the gate-to-source leakage current with the drain terminal shorted to the source terminal. It is given for a specific value of gate reverse-bias voltage. Typical value of gate leakage current is few nanoamperes for JFETs and few pico-amperes for MOSFETs.
6. **Forward Transconductance (g_{fs}):** It is usually given for specified values of gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}). It is typically few hundred micro-mhos to few milli-mhos for both JFETs and MOSFETs.
7. **Output Conductance (g_{os}):** It is the reciprocal of the dynamic drain resistance (r_d). It is usually specified as an admittance parameter (y_{os}). y_{os} equals g_{os} at low frequencies. Admittance is in the range of few milli-mhos for both JFETs and MOSFETs.
8. **Input Capacitance (C_{iss}):** It is the input capacitance of the FET when connected in common-source configuration. It is typically of the order of few picofarads for both JFET and MOSFET devices. The overall input capacitance (C_i) in a common-source amplifier configuration using an FET is larger than C_{iss} due to the presence of Miller component of the gate-drain inter-electrode capacitance (C_{gd} or C_{rss}). C_{gd} is also referred to as the reverse transfer capacitance. The overall input capacitance is given by:

$$C_i = C_{iss} + (1 - A_V)C_{rss} \tag{5.11}$$

where A_V is the voltage gain.

9. **Reverse Transfer Capacitance (C_{rss}):** It is the reverse transfer capacitance for the common-source configuration. It is of the order of few picofarads in JFETs but only a small fraction of a picofarad in some MOSFETs.
10. **Output Capacitance (C_{oss}):** It is the drain-source capacitance for the common-source configuration. This too is typically few picofarads for both JFET and MOSFET devices.
11. **Threshold Voltage ($V_{GS(th)}$):** It is the gate-source threshold voltage where the MOSFET begins to conduct. It is specified for E-MOSFETs only.
12. **Drain-Source ON Voltage ($V_{DS(on)}$):** It is the drain-source voltage for a particular level of gate-source voltage and drain current when the MOSFET is in the ON-state. It is specified for E-MOSFETs only.
13. **ON-State Drain Current ($I_{D(on)}$):** It is a typical value of drain current for a particular value of gate-source voltage when the MOSFET is in the ON-state. It is specified for E-MOSFETs only. As mentioned earlier, the drain current in an E-MOSFET is given by

$$I_D = K(V_{GS} - V_T)^2$$

Therefore, the values of V_T, $V_{GS(on)}$ and $I_{D(on)}$ help in determining the value of K. The value of K is given by

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \tag{5.12}$$

5.5 Differences between JFETs and MOSFETs

JFETs and MOSFETs are somewhat similar devices but there are quite a few differences between the two devices in terms of their principle of operation and the values of their characteristic parameters. These differences are as follows:

1. JFETs are operated in depletion mode only. DE-MOSFETs can be operated in both depletion and enhancement modes and E-MOSFETs are operated in enhancement mode only.
2. The input resistance offered by MOSFETs is much higher than that by JFETs. Input resistance for JFETs is greater than 10^9 Ω whereas that of MOSFETs is around 10^{13} Ω.
3. JFETs have higher drain resistance than MOSFETs and hence their characteristic curve is more flat than that of MOSFETs. Drain resistance for JFETs is in the range of 100 kΩ to 1 MΩ while that for MOSFETs is in the range of 1 to 50 kΩ.
4. The leakage gate current in MOSFETs is much smaller than that in JFETs. The gate current for the MOSFETs is in the range of 100 nA to 10 pA whereas that for the JFETs is in the range of 100 μA to 10 nA.
5. MOSFETs are easier to construct and are used more widely than JFETs.

5.6 Handling MOSFETs

Owing to the presence of thin SiO_2 layer in MOSFETs, they are prone to damage if not handled properly. A person accumulates static charge from the surroundings. When that person handles a MOSFET device, that charge can lead to potential difference across the SiO_2 layer which can result in its breakdown and establish conduction through it. Therefore, some precautions need to be taken while handling MOSFETs.

A shorting conducting foil or a shorting ring is connected across all the three leads of the device until the device is inserted into the system. The shorting ring prevents the development of potential difference between any two device terminals. The person using the MOSFET should always touch ground before using the device so as to discharge the accumulated charge before handling the device. The person who is soldering should use a shorting strap to discharge static electricity and also should make sure that the tip of the soldering iron is grounded. Also the MOSFET should always be held from the casing. In addition, the MOSFET should be inserted or removed with the supply off.

An effective method to prevent MOSFET damage is to connect Zener diodes back-to-back between the gate and the source terminals so that the gate-to-source voltage never exceeds the specified maximum rating. Figure 5.26 shows the use of Zener diodes for protection of E-MOSFETs. Similar configuration can be used

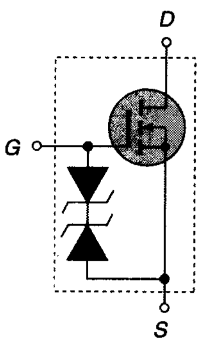


Figure 5.26 | Use of Zener diodes to protect E-MOSFET.

for DE-MOSFETs. But the use of Zener diodes results in reduction of input impedance as the impedance of the Zener diode in the reverse-bias mode is less than the input impedance of the MOSFET.

5.7 Biasing JFETs

DC biasing of an FET is done to produce the required gate-to-source voltage (V_{GS}) to get the desired value of drain current (I_D). There are large variations in the maximum and the minimum values of FET parameters even for a given type. The biasing circuits should maintain the drain current and the drain-source voltage within reasonable limits even for the maximum and minimum values of its parameters. It may be mentioned here that the phenomenon of thermal runaway does not occur in FETs. In this section, we discuss the common configurations used for biasing JFETs. The biasing configurations for DE-MOSFETs and E-MOSFETs are discussed in the next section. There are three biasing configurations used with JFETs, namely, the common-source, common-drain and common-gate configurations. Each of these configurations is discussed in the subsequent paragraphs.

Common-Source Configuration

Common-source configuration offers high input impedance, low output impedance, high voltage gain and the output voltage is 180° out-of-phase with the input voltage. The commonly used common-source biasing configurations include fixed-bias configuration, self-bias configuration and voltage-divider configuration.

Fixed-Bias Configuration

Fixed-bias configuration is the most simplest of the biasing configurations. Figure 5.27 shows the fixed-bias circuit for N-channel JFET. The biasing components include drain resistor (R_D), gate resistor (R_G), input and output coupling capacitors (C_i and C_o), drain supply voltage (V_{DD}) and gate supply voltage (V_{GG}). The gate supply voltage ensures that the gate terminal is negative w.r.t. to the source. Resistor R_G is used so that the input AC signal develops across it. The DC equivalent of the circuit is shown in Figure 5.28.

In a JFET, the gate current (I_G) is approximately equal to zero ($I_G \cong 0$). Therefore, the voltage drop across the resistor R_G, given by the product of the gate current and resistor R_G, is approximately zero.

$$V_{R_G} = I_G \times R_G \cong 0 \tag{5.13}$$

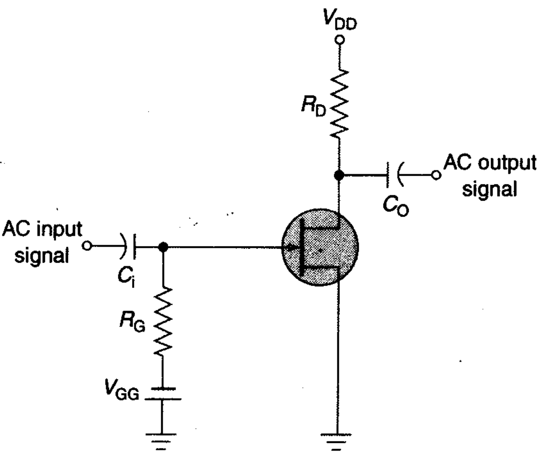


Figure 5.27 | Fixed-bias circuit for N-channel JFET.

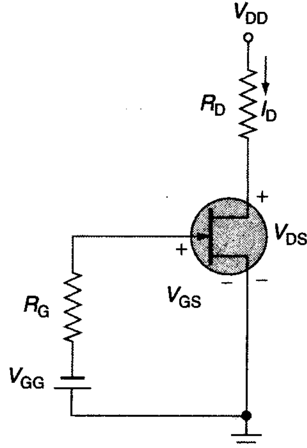


Figure 5.28 | DC equivalent of fixed-bias circuit of Figure 5.27.

Applying Kirchhoff's voltage law to the input section we get

$$-V_{GG} - V_{GS} = 0 \tag{5.14}$$

Therefore, the value of gate-source voltage is given by

$$V_{GS} = -V_{GG} \tag{5.15}$$

The gate-source voltage (V_{GS}) is negative and equal in magnitude to the applied gate voltage (V_{GG}). As the voltage V_{GG} is fixed, V_{GS} is also fixed. Therefore, the configuration is named as fixed-bias configuration. This value of gate-source voltage is denoted as V_{GSQ}.

Since the drain current (I_D) in a JFET is given by Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Therefore, the value of quiescent drain current (I_{DQ}) is given by

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2 \tag{5.16}$$

Since the value of gate-source voltage (V_{GS}) in a fixed-bias configuration is fixed, therefore the level of drain current (I_D) is also fixed.

Applying Kirchhoff's voltage law to the output section we get

$$V_{DD} - I_D R_D - V_{DS} = 0 \tag{5.17}$$

Therefore, the value of quiescent drain-source voltage (V_{DSQ}) is given by

$$V_{DSQ} = V_{DD} - I_{DQ} R_D \tag{5.18}$$

The operating point is defined as (I_{DQ}, V_{DSQ}). The operating point can also be obtained graphically, by superimposing the vertical line $V_{GS} = -V_{GG}$ on the transfer characteristics of the JFET (Figure 5.29).

The operating point can also be obtained by superimposing the load line on the output characteristic curves of the JFET. The load line is defined by Eq. (5.17).

Substituting $V_{DS} = 0$ in Eq. (5.17), we get $I_D = V_{DD}/R_D$
Substituting $I_D = 0$ in Eq. (5.17), we get $V_{DS} = V_{DD}$

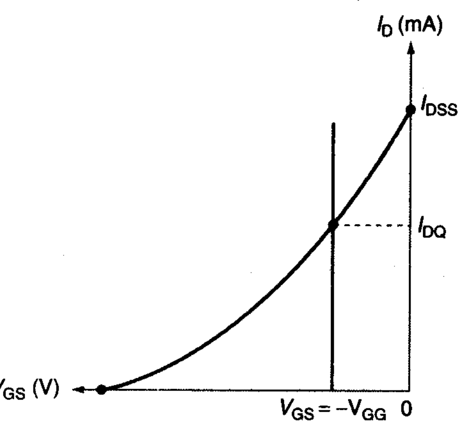


Figure 5.29 | Graphical analysis of the fixed-bias circuit of Figure 5.27.

The line formed by joining the two points (0, V_{DD}) and (V_{DD}/R_D, 0) is the DC load line. As we have studied in the chapter on BJT biasing, the operating point defines the DC conditions that exist when no input AC signal is applied. The bias point is selected so as to have the maximum possible drain-source voltage swing for the AC input signal. Figure 5.30 shows the load-line analysis.

The fixed-bias configuration is not used much as the wide differences in the minimum and maximum values of the JFET parameters make drain current levels unpredictable with simple fixed-bias circuits. Another disadvantage of the fixed-bias circuit is that it needs an additional supply voltage for biasing the gate terminal. Self-bias and potential-divider biasing configurations require a single supply voltage and maintain the quiescent drain current and drain-source voltage within desirable limits.

Self-Bias Configuration

Self-bias configuration is the most commonly used biasing scheme for FETs. Self-bias configuration offers stabilization of the operating point against variations in FET parameters. Figure 5.31 shows the self-bias circuit for an N-channel JFET. The difference between the fixed-bias and the self-bias configurations is the

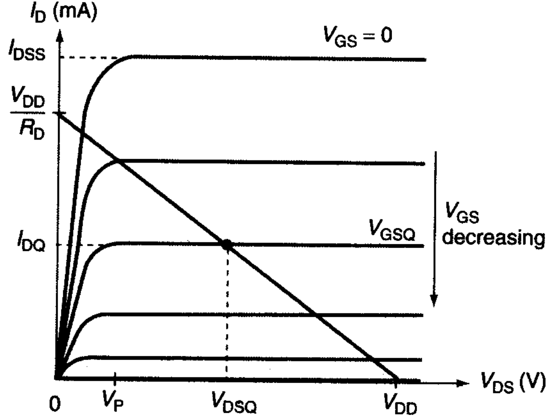


Figure 5.30 | Load-line analysis for the fixed-bias circuit of Figure 5.27.

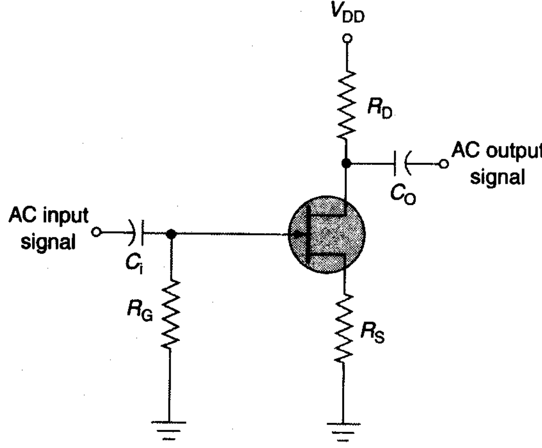


Figure 5.31 | Self-bias configuration for N-channel JFET.

addition of source resistor (R_S) between the source and the ground terminals and the removal of the gate supply voltage. The voltage drop across the resistor (R_S) provides the controlling gate voltage.

The analysis of the self-bias circuit can be done by drawing its DC equivalent circuit as shown in Figure 5.32. As the gate current (I_G) is zero, there is no voltage drop across the resistor R_G. Therefore the gate voltage V_G is equal to zero. Applying Kirchhoff's voltage law to the input section we get

$$-V_{GS} - I_D R_S = 0 \tag{5.19}$$

Therefore, the gate-source voltage is given by

$$V_{GS} = -I_D R_S \tag{5.20}$$

As the gate voltage is zero, the source voltage (V_S) is given by

$$V_S = V_G - V_{GS} = I_D R_S \tag{5.21}$$

The voltage drop (V_S) across source resistor R_S provides the biasing gate-source voltage and hence no external power supply is required for the purpose. Hence this configuration is named self-bias configuration. The voltage (V_S) also results in bias-point stabilization. If the transconductance of the JFET decreases, the drain current decreases resulting in decrease in the voltage across resistor R_S. Thus the voltage V_{GS} becomes less negative resulting in increase in drain current. This compensates for the initial decrease in the drain current.

Drain current (I_D) in a JFT is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Substituting the value of V_{GS} in the expression for drain current (I_D) we get

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2 \tag{5.22}$$

Therefore, the drain current is given by

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2 \tag{5.23}$$

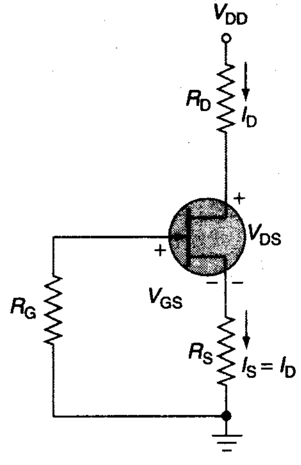


Figure 5.32 | DC equivalent of self-bias configuration shown in Figure 5.31.

Applying Kirchhoff's voltage law to the output section we get

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0 \tag{5.24}$$

Therefore, the drain-source voltage (V_{DS}) is given by

$$V_{DS} = V_{DD} - I_D (R_D + R_S) \tag{5.25}$$

The graphical analysis can be done in a similar manner to that for fixed-bias configuration as shown in Figure 5.33. The operating point is determined by superimposing the straight line corresponding to the equation $V_{GS} = -I_D R_S$ on the transfer characteristic curve of the JFET. The load-line analysis can also be done in the same manner as done for the fixed-bias circuit. The only difference is that the load line is now defined by Eq. (5.25).

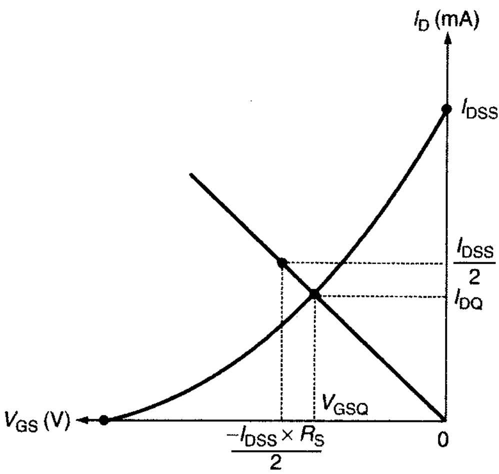


Figure 5.33 | Graphical analysis of self-bias configuration for N-channel JFETs.

EXAMPLE 5.4 *For the self-bias circuit in Figure 5.34, determine the value of drain current (I_D) and gate-source voltage (V_{GS}).*

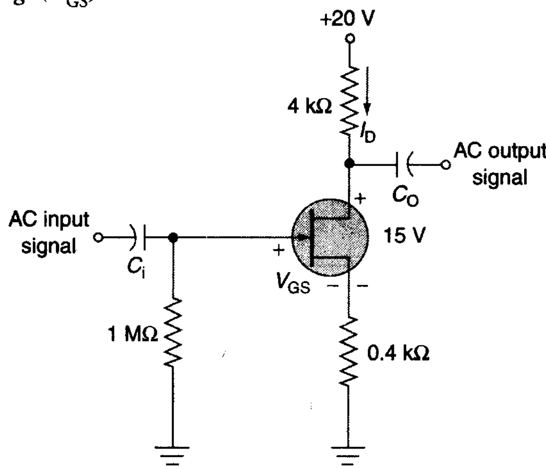


Figure 5.34 | Example 5.4.

Solution

1. The value of drain current is given by

$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S}$$

2. Therefore, $I_D = (20 - 15)/(4 \times 10^3 + 0.4 \times 10^3) = 5/4.4 \times 10^3 = 1.14$ mA.
3. The gate-source voltage is given by $V_{GS} = -I_D \times R_S = -1.14 \times 10^{-3} \times 0.4 \times 10^3 = 0.456$ V.

Answer: Drain current $I_D = 1.14$ mA and gate-source voltage $V_{GS} = 0.456$ V.

Voltage-Divider Biasing

Voltage-divider biasing configuration used in the case of BJTs is also applicable to JFETs. As mentioned in Chapter 4 on BJT biasing, the voltage-divider configuration offers improved bias stability. The voltage-divider biasing configuration for N-channel JFET is shown in Figure 5.35. The resistors R_1 and R_2 form the potential divider. Voltage across resistor R_2 provides the necessary bias to the JFET. Figure 5.36 shows the DC equivalent of the configuration.

As the gate current $I_G \cong 0$, the gate voltage is given by

$$V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2} \tag{5.26}$$

The gate-source voltage (V_{GS}) is given by

$$V_{GS} = V_G - V_S = V_G - I_D R_S \tag{5.27}$$

As the gate-source voltage should be negative for proper operation of N-channel JFETs, therefore for the circuit to operate properly the voltage ($I_D \times R_S$) should be larger than voltage V_G.

Applying Kirchhoff's voltage law to the output section we get

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \tag{5.28}$$

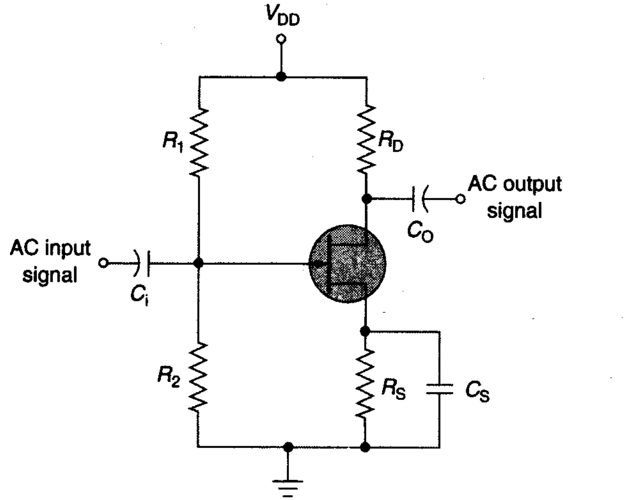


Figure 5.35 Voltage-divider biasing configuration for N-channel JFET.

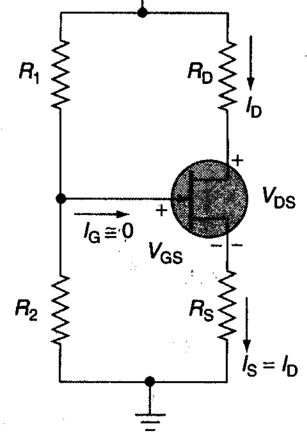


Figure 5.36 DC equivalent of voltage-divider biasing configuration of Figure 5.35.

The operating point is given by

$$\left(I_{DQ} = \frac{V_G - V_{GS}}{R_S},\ V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)\right)$$

Figure 5.37 shows the graphical method to determine the operating point. The figure is self-explanatory. Load-line analysis can also be done to establish the operating point as explained in the case of fixed-bias circuit.

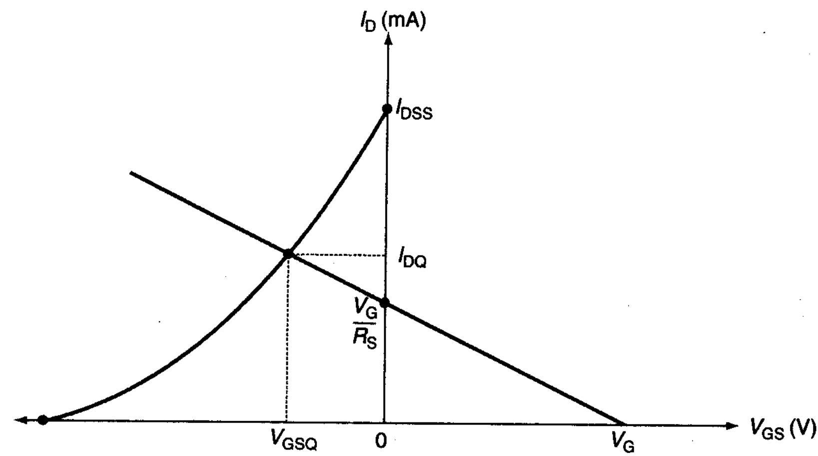


Figure 5.37 | Graphical analysis of voltage-divider bias configuration.

EXAMPLE 5.5 *For the circuit in Figure 5.38, determine the value of drain-source voltage (V_{DS}). (Given that the gate-source voltage is −0.8 V.)*

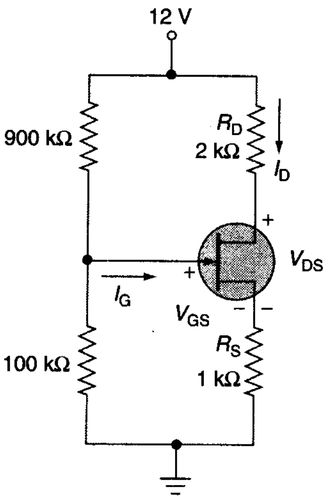


Figure 5.38 | Example 5.5.

Solution

1. The gate voltage is given by $V_G = 12 \times 100 \times 10^3/(100 \times 10^3 + 900 \times 10^3) = 1.2$ V.

2. The gate-source voltage is equal to $V_{GS} = V_G - V_S$.
   Therefore, $-0.8 = 1.2 - V_S$ or $V_S = 2.0$ V.
3. The drain current is equal to $I_D = V_S/R_S = 2/(1 \times 10^3) = 2$ mA.
4. The drain-source voltage is $V_{DS} = 12 - 2 \times 10^3 \times 2 \times 10^{-3} - 1 \times 10^3 \times 2 \times 10^{-3}$ $= 12 - 4 - 2 = 6$ V.

Answer: The drain-source voltage is equal to 6 V.

Common-Drain Configuration

The basic circuit for the common-drain configuration or the source follower configuration is shown in Figure 5.39. As is evident from the figure, no resistor is connected in series with the drain terminal. The voltage across resistor R_S provides the gate-source biasing voltage. The output is taken from the source terminal. This configuration is similar to the common-collector configuration for the BJTs. Like the common-collector configuration, the common-drain configuration also offers high input impedance, low output impedance, nearly unity voltage gain and no input–output phase reversal. The DC equivalent of the circuit in Figure 5.39 is shown in Figure 5.40.

As the gate current (I_G) is approximately equal to zero, the gate voltage V_G is also equal to zero. Applying Kirchhoff's voltage law to the input section we get

$$-V_{GS} - I_D R_S = 0$$

Therefore, the gate-source voltage is given by

$$V_{GS} = -I_D R_S \tag{5.29}$$

As the gate voltage is zero, the source voltage (V_S) is given by

$$V_S = I_D R_S \tag{5.30}$$

Applying Kirchhoff's voltage law to the output circuit we get

$$V_{DD} - V_{DS} - I_D R_S = 0$$

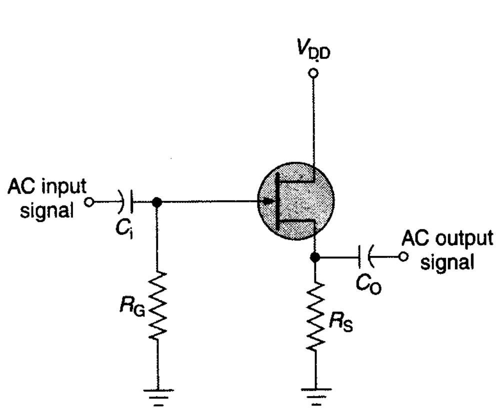


Figure 5.39 Common-drain configuration for N-channel JFET.

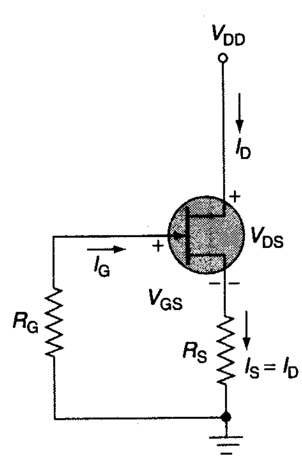


Figure 5.40 DC equivalent of the common-drain configuration of Figure 5.39.

Therefore, the drain-source voltage is given by

$$V_{DS} = V_{DD} - I_D R_S \tag{5.31}$$

Another possible common-drain configuration is shown in Figure 5.41(a). This configuration is based on the boot-strapped bias configuration and provides increased input resistance. The concept of boot-strapping is discussed in detail in Chapter 8. Figure 5.41(b) shows the voltage-divider common-drain amplifier. The gate-bias voltage V_G is derived from V_{DD} by means of potential divider formed by resistors R_1 and R_2. In this case also, no resistor is connected in series with the drain terminal. The analysis for both the circuits can be done on similar lines as outlined earlier.

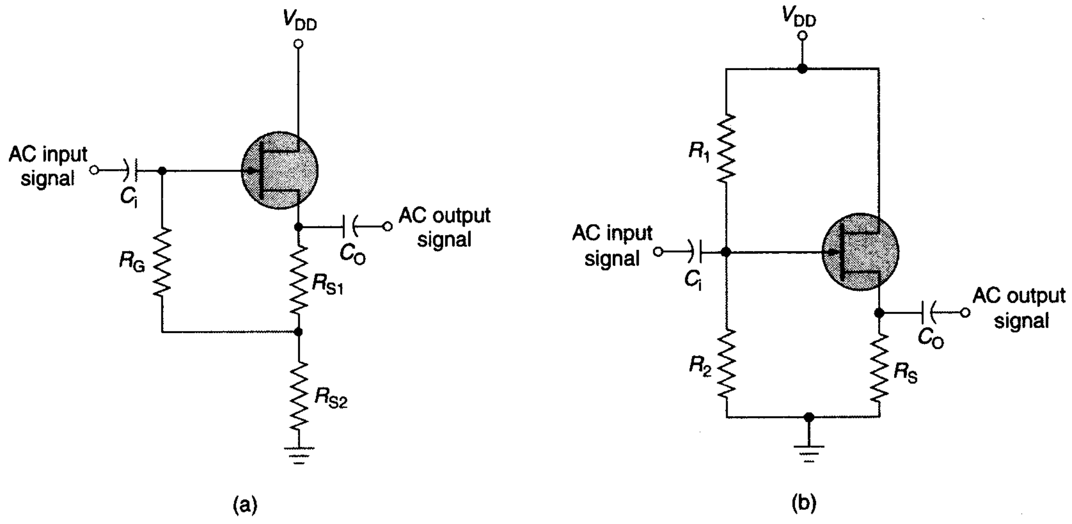


Figure 5.41 (a) Common-drain configuration with boot-strapping for N-channel JFET; (b) voltage-divider common-drain configuration for N-channel JFET.

EXAMPLE 5.6 *In an N-channel JFET-based voltage-divider common-drain configuration, determine the value of resistor (R_S) so as to have the operating point as I_{DQ} = 5 mA, V_{DSQ} = 10 V. Given that V_{DD} = 28 V, R_1 = 1 MΩ, R_2 = 0.5 MΩ, saturation drain current of the JFET = 10 mA and gate-source pinch-off voltage = −5 V.*

Solution

1. In a JFET,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$5 \times 10^{-3} = 10 \times 10^{-3}\ [1 - V_{GS}/(-5)]^2$$

$$V_{GS} = -1.5\ \text{V}$$

2. In the voltage-divider configuration,

$$V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2}$$

$$V_G = 0.5 \times 10^6 \times 28/(0.5 \times 10^6 + 1 \times 10^6) = 28/3 = 9.33 \text{ V}$$

3. The value of the resistance R_S is given by

$$R_S = \frac{(V_G - V_{GS})}{I_D}$$

$$R_S = [9.33 - (-1.5)]/5 \times 10^{-3} = 2.166 \text{ k}\Omega$$

Answer: The value of the resistor R_S is 2.166 kΩ.

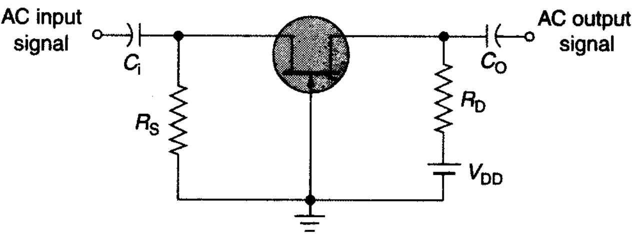


Figure 5.42 | Common-gate configuration for N-channel JFET.

Common-Gate Configuration

Figure 5.42 shows the common-gate configuration for an N-channel JFET. The input is applied between the source and the gate terminals and the output is taken between the drain and the gate terminals. Common-gate configuration offers low input impedance, high output impedance, high voltage gain and the output voltage is in phase with the input voltage. The analysis for the circuit can be done on similar lines as that outlined earlier. The values of the gate-source and drain-source voltages are given by Eqs. (5.32) and (5.33), respectively.

$$V_{GS} = -I_D R_S \tag{5.32}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D) \tag{5.33}$$

5.8 Biasing MOSFETs

In this section we will discuss the commonly used biasing configurations for the DE-MOSFETs and the E-MOSFETs.

Depletion MOSFETs

The biasing schemes for DE-MOSFETs are the same as that for JFETs because of the similarities in their characteristics. The only difference being that DE-MOSFETs also operate in enhancement mode, that is, with positive values of gate-source voltage (V_{GS}) in addition to the depletion mode. The operation of the DE-MOSFET in the enhancement mode is explained with the help of Example 5.7.

EXAMPLE 5.7 | *Figure 5.43 shows a biasing configuration using DE-MOSFET. Given that the saturation drain current is 8 mA and the pinch-off voltage is −2 V, determine the value of gate-source voltage, drain current and the drain-source voltage.*

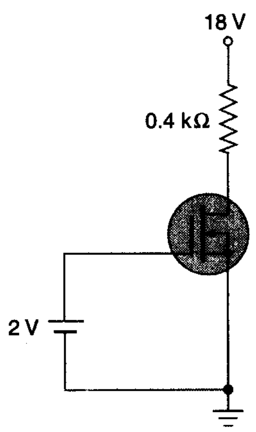


Figure 5.43 | Example 5.7.

Solution

1. The gate-source voltage (V_{GS}) is equal to 2 V.
2. The polarity of the voltage applied between the gate and the source terminals is such that the MOSFET operates in the enhancement region of its output characteristics.
3. In a DE-MOSFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Now $I_{DSS} = 8$ mA, $V_{GS} = 2$ V, $V_P = -2$ V. Substituting in the above equation we get

$$I_D = 8 \times 10^{-3} \times [1-2/(-2)]^2 = 32 \times 10^{-3}\ \text{A} = 32\ \text{mA}$$

4. Applying Kirchhoff's voltage law to the output section we get

$$18 - 0.4 \times 10^3 \times 32 \times 10^{-3} - V_{DS} = 0$$

$$V_{DS} = 18 - 12.8 = 5.2\ \text{V}$$

Answer: Gate-source voltage = 2 V, drain current = 32 mA, drain-source voltage = 5.2 V.

EXAMPLE 5.8

Design a voltage-divider-bias network using a DE-MOSFET with supply voltage V_{DD} = 16 V, I_{DSS} = 10 mA and $V_P = -5$ V to have a quiescent drain current of 5 mA and gate voltage of 4 V. (Assume the drain resistor R_D to be four times the source resistor R_S.)

Solution

1. As the quiescent drain current is less than saturation drain current, the MOSFET is operated in the depletion mode.
2. The drain current (I_D) is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$5 \times 10^{-3} = 10 \times 10^{-3} \times [1 - \{V_{GS} /(-5)\}]^2$$
$$0.5 = (1 + V_{GS} /5)^2$$
$$V_{GS} / 5 = 0.7 - 1 = -1.5 \text{ V}$$

3. The gate-source voltage (V_{GS}) is given by $V_{GS} = V_G - V_S = V_G - I_D R_S$.
4. $I_D \times R_S = 4 + 1.5 = 5.5$ V.
5. $R_S = 5.5/5 \times 10^{-3} = 1.1$ kΩ.
6. $R_D = 4 \times R_S = 4 \times 1.1 \times 10^3 = 4.4$ kΩ.
7. $V_G = [R_2/(R_1 + R_2)] \times 16$.
8. Let us assume $R_2 = 1$ kΩ. Therefore,
   $4 = 16 \times 1 \times 10^3/(R_1 + 1 \times 10^3)$
   $(R_1 + 1 \times 10^3) = 4 \times 10^3$ or $R_1 = 3 \times 10^3 = 3$ kΩ
9. Figure 5.44 shows the circuit configuration.

Answer: Figure 5.44 shows the voltage-divider configuration.

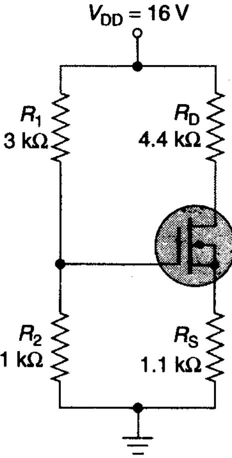


Figure 5.44 | Solution to Example 5.8.

Enhancement MOSFETs

Two most popular biasing configurations for E-MOSFETs are the feedback biasing configuration and the voltage-divider configuration. These two biasing configurations are described in this section.

Feedback-Biasing Configuration

Figure 5.45 shows the circuit for the feedback-biasing configuration. The feedback connection to the gate terminal is taken from the drain terminal through resistor R_G. The resistor R_G brings bias voltage to the gate terminal to turn the MOSFET ON. Figure 5.46 shows the DC equivalent circuit. Since the gate current (I_G) is approximately equal to zero, therefore the voltage drop across resistor R_G is also approximately equal to zero. Applying Kirchhoff's voltage law to the input section we get

$$V_{DD} - I_D R_D - V_{GS} = 0 \tag{5.34}$$

Therefore, gate-source voltage (V_{GS}) is given by

$$V_{GS} = V_{DD} - I_D R_D \tag{5.35}$$

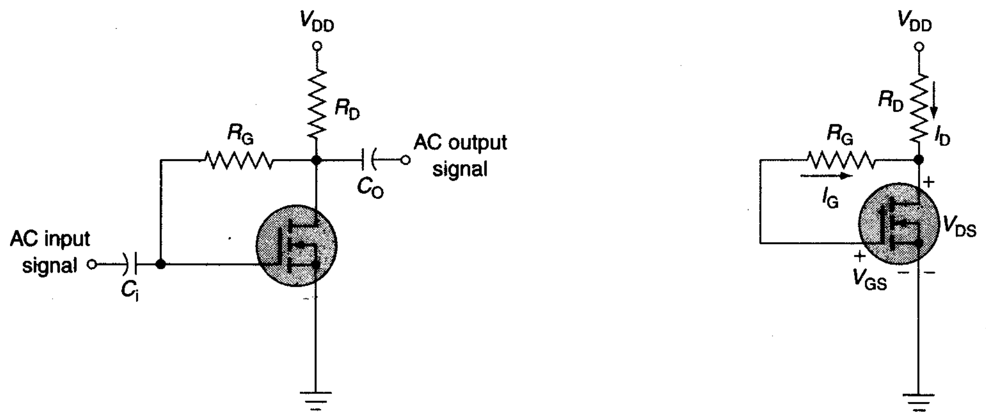


Figure 5.45 | Feedback-biasing configuration for N-channel E-MOSFET.

Figure 5.46 | DC equivalent of the circuit.

Applying Kirchhoff's voltage law to the output section and solving for the drain-source voltage (V_{DS}) we get

$$V_{DS} = V_{DD} - I_D R_D \tag{5.36}$$

It is clear from Eqs. (5.35) and (5.36) that the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}) are equal, that is,

$$V_{GS} = V_{DS} \tag{5.37}$$

The operating point is given by (I_{DQ}, V_{DSQ}). The operating point can also be established using graphical method as shown in Figure 5.47. The figure shows that the straight line given by Eq. (5.35) is superimposed on the transfer characteristics of the MOSFET. The point of intersection between the straight line and the transfer curve gives the value of the quiescent gate-source voltage and quiescent drain current. The operating point can also be obtained by superimposing the DC load line defined by Eq. (5.36) on the output characteristic curves for the MOSFET.

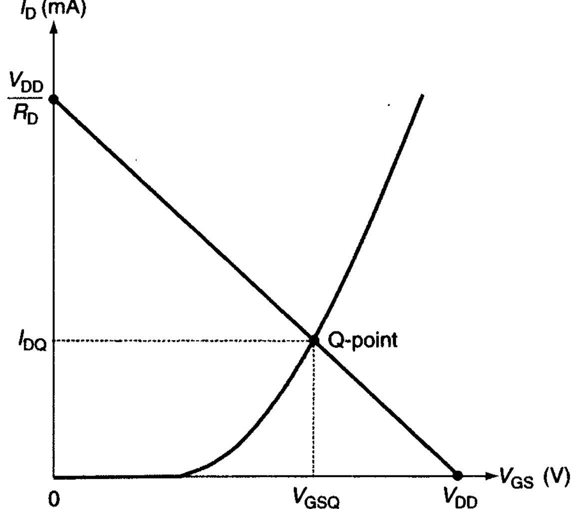


Figure 5.47 | Graphical method for determining the operating point for the circuit in Figure 5.45.

EXAMPLE 5.9

Figure 5.48 shows a circuit using E-MOSFET. Given that the threshold voltage for the MOSFET is 2 V and $I_{D(on)} = 6$ mA for $V_{GS(on)} = 5$ V, determine the value of the operating point.

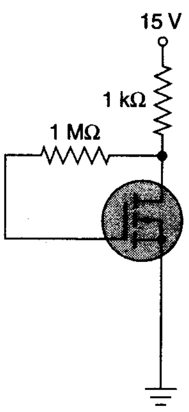


Figure 5.48 | Example 5.9.

Solution

1. Drain current in an E-MOSFET is given by
$$I_D = K(V_{GS} - V_T)^2$$
2. Therefore, $K = 6 \times 10^{-3}/(5 - 2)^2 = 0.67 \times 10^{-3}$ A/V $= 0.67$ mA/V.
3. Gate-source voltage in the feedback configuration is given by
$$V_{GS} = V_{DD} - I_D R_D$$
$$V_{GS} = 15 - I_D \times 1 \times 10^3 = 15 - 1000 I_D$$
4. Substituting this value of I_D in the expression $I_D = K(V_{GS} - V_T)^2$ we get
$$I_D = 0.67 \times 10^{-3}\,(15 - 1000 I_D - 2)^2$$
$$I_D = 0.67 \times 10^{-3}\,(13 - 1000 I_D)^2$$
$$3000 I_D = 2(169 - 26000 I_D + 10^6 I_D^2)$$
$$2 \times 10^6 I_D^2 - 55000 I_D + 338 = 0$$
5. Solving for I_D we get $I_D = 9.3 \times 10^{-3}$ A $= 9.3$ mA.
6. The value of the drain-source voltage (V_{DS}) is given by
$$V_{DS} = V_{DD} - I_D R_D$$
$$V_{DS} = 15 - 9.3 \times 10^{-3} \times 1 \times 10^3$$
$$= 15 - 9.3 = 5.7 \text{ V}$$

Answer: The operating point is given by (9.3 mA, 5.7 V).

Voltage-Divider-Biasing Configuration

Voltage-divider-biasing configuration is another popular biasing arrangement with E-MOSFETs. Figure 5.49 shows the biasing configuration. The arrangement is the same as that for BJTs and JFETs. The DC equivalent circuit is shown in Figure 5.50. The analysis can be done in a manner similar to that done in the case of JFETs.

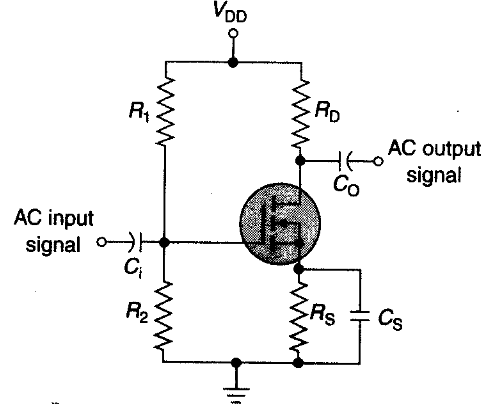


Figure 5.49 Voltage-divider-biasing configuration for N-channel E-MOSFET.

Figure 5.50 DC equivalent of the voltage-divider-biasing configuration in Figure 5.49.

EXAMPLE 5.10

Figure 5.51 shows a voltage-divider configuration for the E-MOSFET. Given that the threshold voltage for the MOSFET is 4 V and the value of $I_{D(on)} = 6$ mA for $V_{GS(on)} = 8$ V, use graphical method to determine the value of the quiescent drain current, gate-source voltage and drain-source voltage.

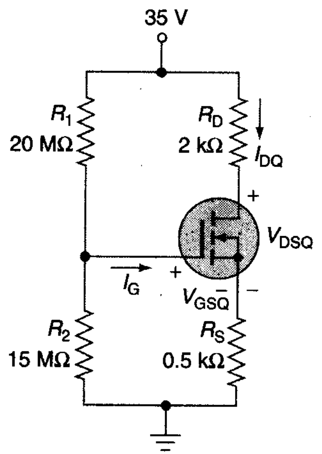


Figure 5.51 Example 5.10.

Solution

1. The transfer characteristics of the MOSFET can be plotted by finding the value of K using

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$

2. Given that $I_{D(on)} = 6$ mA, $V_{GS(on)} = 8$ V and $V_{GS(th)} = 4$ V, therefore

$$K = 6 \times 10^{-3}/(8-4)^2 = 0.375 \times 10^{-3} \text{ A/V}^2$$

3. Therefore, the value of drain current is given by

$$I_D = 0.375 \times 10^{-3} (V_{GS} - V_{GS(th)})^2$$

4. For $V_{GS} = 5$ V, $I_D = 0.375$ mA; for $V_{GS} = 7.5$ V, $I_D = 4.59$ mA; for $V_{GS} = 10$ V, $I_D = 13.5$ mA; for $V_{GS} = 12.5$ V, $I_D = 27.09$ mA and for $V_{GS} = 15$ V, $I_D = 45.375$ mA.
5. The transfer curve can be plotted using these values of V_{GS} and I_D. Figure 5.52(a) shows the transfer characteristics of the MOSFET.

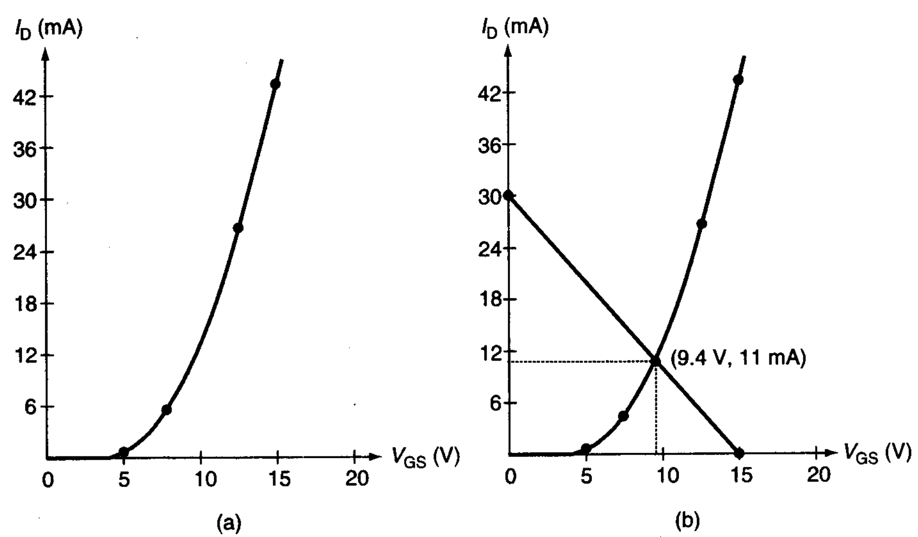


Figure 5.52 | Solution to Example 5.10.

6. The next step is to draw the load line.
7. The gate voltage (V_G) is given by

$$V_G = \frac{R_2 \times V_{DD}}{R_1 + R_2}$$

$$V_G = 15 \times 10^6 \times 35/(20 \times 10^6 + 15 \times 10^6) = 15 \text{ V}$$

8. The gate-source voltage (V_{GS}) is given by

$$V_{GS} = V_G - V_S = V_G - I_D R_S$$

9. For $I_D = 0$, $V_{GS} = 15$ V
10. For $V_{GS} = 0$, $I_D = 15/0.5 \times 10^3 = 30$ mA
11. The next step is to draw the load line with coordinates (0, 15 V) and (30 mA, 0) on the transfer characteristics [Figure 5.52(b)].
12. From Figure 5.52(b), the quiescent values of gate-source voltage and drain current are 9.4 V and 11 mA respectively.
13. The value of the drain-source voltage is given by

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_{DS} = 35 - 11 \times 10^{-3} (2 \times 10^3 + 0.5 \times 10^3) = 35 - 11 \times 2.5 = 7.5 \text{ V}$$

Answer: The quiescent values of drain-source voltage, gate-source voltage and drain current are 7.5 V, 9.4 V and 11 mA, respectively.

EXAMPLE 5.11 *Determine the values of voltages V_D and V_C for the circuit shown in Figure 5.53, given that the transistor β is 100, V_{BE} = 0.7V, saturation drain current of JFET is 10 mA and the pinch-off voltage is −5 V.*

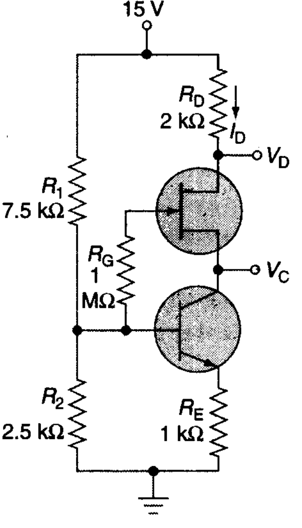


Figure 5.53 | Example 5.11.

Solution

1. The figure shows the voltage-divider transistor configuration with an additional JFET connected between the base and the collector terminals.
2. Value of $\beta \times R_E = 100 \times 1 \times 10^3 = 10^5$.
   Value of $10 \times R_2 = 10 \times 2.5 \times 10^3 = 2.5 \times 10^4$.
3. As the value of $(\beta \times R_E)$ is much larger than $(10 \times R_2)$, approximate analysis can be done to analyze the voltage-divider transistor configuration.
4. $V_B = 15 \times 2.5 \times 10^3/(2.5 \times 10^3 + 7.5 \times 10^3) = 3.75$ V.
5. $V_E = V_B - V_{BE} = 3.75 - 0.7 = 3.05$ V.
6. $I_E = V_E/R_E = 3.05/(1 \times 10^3) = 3.05$ mA.
7. $I_C \cong I_E = 3.05$ mA.
8. In the figure shown, $I_D = I_S = I_C = 3.05$ mA.
9. The drain voltage (V_D) is equal to $V_D = 15 - I_D \times 2 \times 10^3$
   $$V_D = 15 - 3.05 \times 10^{-3} \times 2 \times 10^3 = 15 - 6.1 = 8.9 \text{ V}$$
10. As the current through the gate resistor is zero, therefore there is no voltage drop across the resistor R_G. The value of collector voltage (V_C) is equal to $V_C = V_B - V_{GS}$.
11. In a JFET the drain current is given by
   $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
   $$3.05 \times 10^{-3} = 10 \times 10^{-3}\ [1 - V_{GS}/(-5)]^2$$
   $$V_{GS} = -2.24 \text{ V}$$
12. Therefore, $V_C = 3.75 - (-2.24) = 5.99$ V.

Answer: $V_C = 5.99$ V, $V_D = 8.9$ V.

5.9 FET Applications

The major shortcoming of BJTs is their low value of input impedance which leads to loading of the input source. As FETs offer very high value of input impedance as compared to BJTs, they are ideal for many applications where BJTs can be used. FETs are widely used as input amplifiers in oscilloscopes, electronic voltmeters and other test and measurement instruments, as low-noise amplifiers in front end of TV and radio receivers. FETs in the common-drain configuration are used as buffer amplifiers. E-MOSFETs are very commonly used in the fabrication of integrated circuits. Another common application of FETs is in switching applications and as voltage-variable resistors (VVRs) in operational amplifiers. Some of the common applications of FETs are discussed in this section.

1. **Amplifiers:** FET devices are commonly used as low-noise amplifiers and as buffer amplifiers. FETs are low-noise devices and hence they are used in the front-end of receivers and other electronic equipments and systems. JFETs in common-drain configuration (source follower) offer high input impedance and low output impedance and hence they are used as buffer amplifiers to isolate the preceding stage from the following stage.
2. **Analog Switch:** FETs are used as analog switches. Figure 5.54 shows one possible switching configuration using an N-channel JFET. When no gate voltage (V_{GG}) is applied, the FET operates in the saturation region and acts as a closed switch. When a negative gate voltage (V_{GG}) is applied, the FET operates in the cut-off region. Therefore, it offers a very high resistance and acts as an open switch.
3. **Multiplexers:** FETs are used in multiplexer circuits where each FET device acts as a single-pole single-throw switch. Figure 5.55 shows an N-channel JFET-based multiplexer. The input signals are applied to the drain terminals of the JFETs while the corresponding control inputs are applied to the gate terminals of the JFETs. When the control input corresponding to one of the input channels is made zero, that input is transmitted to the output. The control inputs for the other channels are made more negative than the $V_{GS(off)}$ voltage. Hence all the other input signals are blocked.
4. **Current Limiters:** FETs can also be used in current-limiting applications as shown in Figure 5.56. During the normal operation of the circuit, the JFET acts in the ohmic region. When the load current increases substantially due to short circuit or any other reason, the JFET operates in the saturation region. Hence it acts as a constant current source and prevents excessive current through the load.
5. **Voltage-Variable Resistors (VVRs):** FETs when operated in the ohmic region (for small positive values of drain-to-source voltage V_{DS}) of their characteristics, act as voltage-variable resistors. In this region the drain

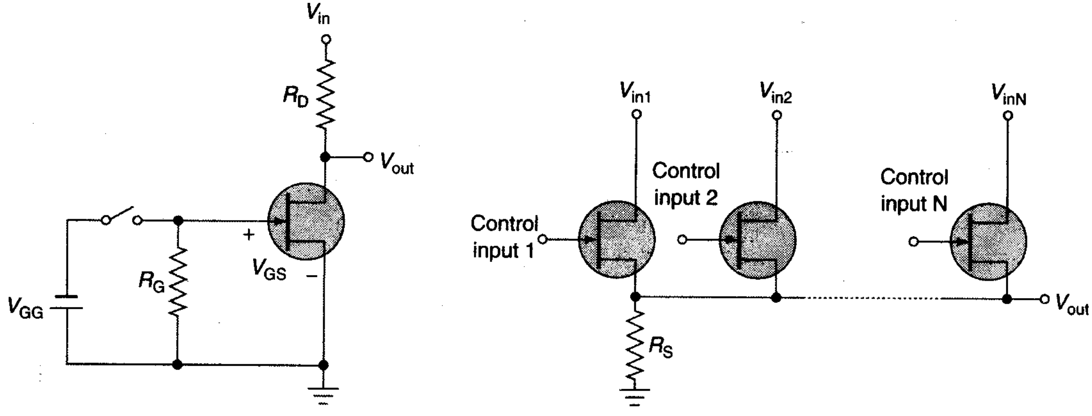


Figure 5.54 | FET as an analog switch.

Figure 5.55 | FET as a multiplexer.

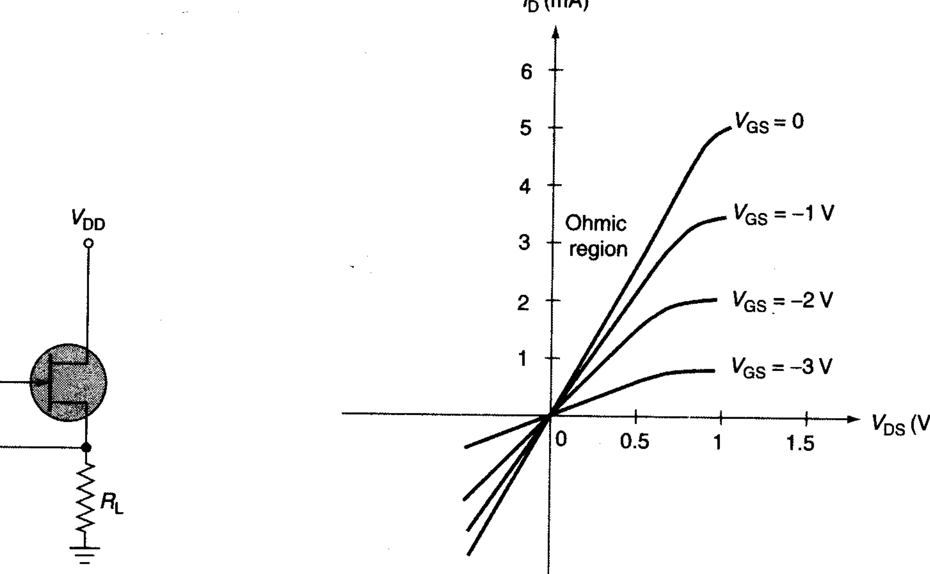


Figure 5.56 | FET for current limiting.

Figure 5.57 | Characteristics of an N-channel JFET in the ohmic region.

resistance R_D can be controlled by the gate-to-source voltage (V_{GS}). For an N-channel JFET, the value of R_D increases with increase in the negative value of V_{GS} as shown in Figure 5.57. As we can see from the figure, the curve is symmetrical near the origin, that is, for small negative values of drain-source voltage the curves are symmetrical to that of positive values of drain-source voltage. Thus, if an AC voltage (with small peak-to-peak voltage) is applied between the drain and the source terminals, then the FET acts as a linear resistor for a given gate-source voltage. FET-based VVRs are used in automatic gain control circuits.

6. **Oscillators:** FETs are also used in phase-shift oscillators (Figure 5.58) and pierce type of crystal-controlled oscillators (Figure 5.59). Oscillators are described in detail in Chapter 12 on sinusoidal oscillators.

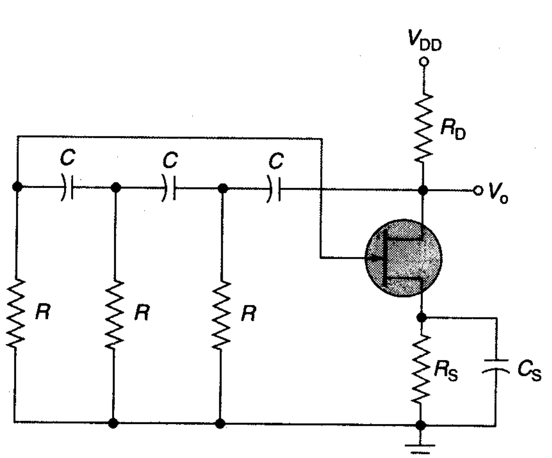


Figure 5.58 | FET-based phase-shift oscillator.

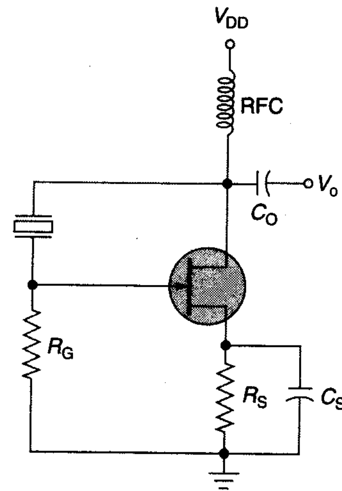


Figure 5.59 | FET-based Pierce oscillator.

EXAMPLE 5.12

The circuit shown in Figure 5.60 uses a JFET in an AGC circuit. The voltage V_C is the control voltage. Derive the expression for the ratio of the output voltage to the input voltage. Also find the value of the output voltage for V_{in} = 5 V when the control voltage V_C is equal to (a) 0 V, (b) 0.5 V_P and (c) V_P. (Given that R_L = 100 kΩ, R = 10 kΩ, the resistance of the JFET at zero gate-source voltage is 10 kΩ.)

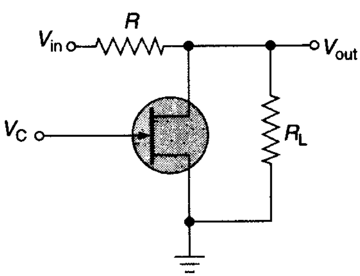


Figure 5.60 | Example 5.12.

Solution

1. If the value of the drain resistance of the FET is R_D then the ratio V_{out} to V_{in} is given by

$$\frac{V_{out}}{V_{in}} = \frac{R_D \| R_L}{(R_D \| R_L) + R} = \frac{R_D \times R_L}{(R_D \times R_L) + R(R_D + R_L)}$$

2. The value of the resistance (R_D) is given by the expression

$$R_D = \frac{R_o}{(1 - V_{GS}/V_P)^2}$$

where R_o is the resistance at $V_{GS} = 0$.

3. The control voltage is applied between the gate and the source terminals, therefore $V_C = V_{GS}$.
4. When $V_C = 0$, $R_D = R_o = 10$ kΩ

$$V_{out} = \frac{5 \times 10 \times 10^3 \times 100 \times 10^3}{(10 \times 10^3 \times 100 \times 10^3) + 10 \times 10^3(10 \times 10^3 + 100 \times 10^3)}$$

$$= \frac{5 \times 1000 \times 10^6}{1000 \times 10^6 + 1100 \times 10^6} = 2.38 \text{ V}$$

5. When $V_C = 0.5\ V_P$, $R_D = 4 \times R_o = 40$ kΩ

$$V_{out} = \frac{5 \times 40 \times 10^3 \times 100 \times 10^3}{(40 \times 10^3 \times 100 \times 10^3) + 10 \times 10^3(40 \times 10^3 + 100 \times 10^3)}$$

$$= \frac{5 \times 4000 \times 10^6}{4000 \times 10^6 + 1400 \times 10^6} = 3.7 \text{ V}$$

6. When $V_C = V_P$, R_D tends to ∞. Therefore

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{R_L + R}$$

$$= 100 \times 10^3/(100 \times 10^3 + 10 \times 10^3) = 0.91$$

$$V_o = 5 \times 0.91 = 4.55\ \text{V}$$

Answer: $\frac{V_{out}}{V_{in}} = \frac{R_D \times R_L}{(R_D \times R_L) + R(R_D + R_L)}$

(a) $V_{out} = 2.38$ V; (b) $V_{out} = 3.7$ V; (c) $V_{out} = 4.55$ V

5.10 Testing FETs

FETs can be checked using a multimeter or an ohmmeter. When an N-channel JFET is checked using a multimeter or an ohmmeter, connecting the red (POSITIVE) lead of the multimeter to the gate terminal and the black (NEGATIVE) lead to the drain terminal should show a low resistance [Figure 5.61(a)]. In this condition, the JFET is checked as a diode (gate-channel junction). By reversing the connections, the meter should show an open circuit (OL indication) or a very high resistance [Figure 5.61(b)]. Also, connecting the red (POSITIVE) lead of the multimeter to the gate terminal and the black (NEGATIVE) lead to the source terminal should show a low resistance [Figure 5.61(c)] and by reversing the connections, the meter should show an open circuit (OL indication) or a very high resistance [Figure 5.61(d)]. If the meter shows a high resistance in both cases, it indicates that the gate junction is open. A low resistance in both cases indicates a shorted gate.

When the meter is connected between the drain and the source terminals, it indicates a small resistance of the order of few hundreds of ohms. The resistance check from the source to the drain [Figure 5.61(e)]

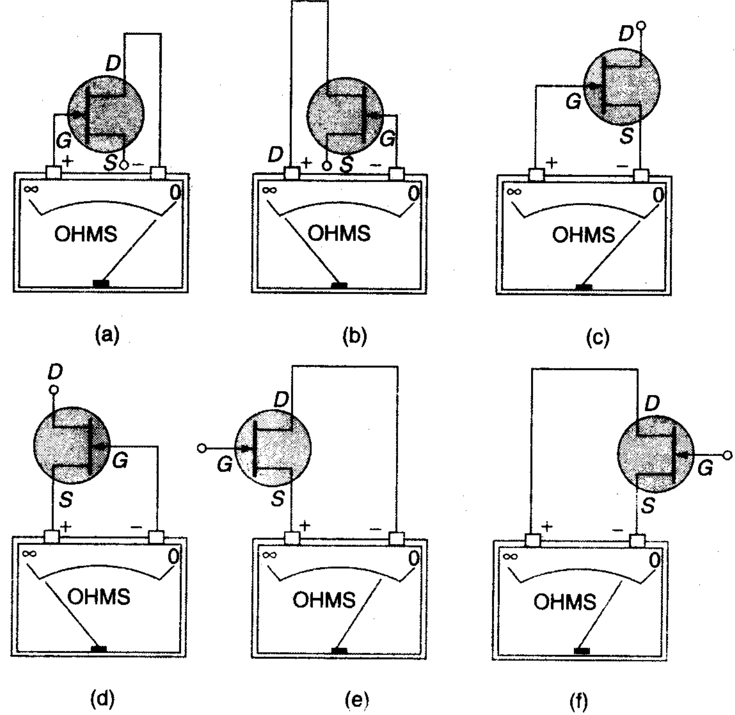


Figure 5.61 | Testing N-channel JFETs with a multimeter.

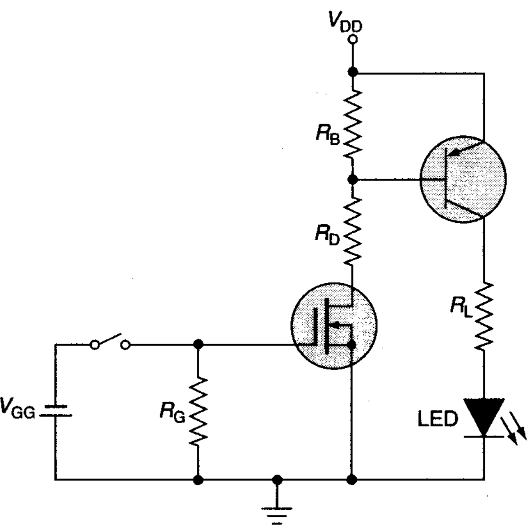


Figure 5.62 | MOSFET test circuit.

should yield similar value as from the drain to the source [Figure 5.61(f)]. While doing the source-drain resistance check, the pins of the JFET should be inserted into an anti-static material prior to testing. This ensures that the residual voltage across the gate-channel PN junction will be neutralized and the test will give accurate results. A P-channel JFET can also be checked in a similar manner.

While checking a MOSFET, the resistance measured between gate and drain terminals should be infinitely high in either direction. Low resistance indicates a faulty device. However, this test does not give complete information about the functioning of the MOSFET. The circuit shown in Figure 5.62 can used to check N-channel DE-MOSFETs. The same circuit can be used to check P-channel E-MOSFETs and N-channel JFETs.

For N-channel DE-MOSFETs and N-channel JFETs when the switch is open, sufficient current flows through resistor R_B to forward-bias the emitter–base junction of the bipolar junction transistor and it starts conducting. The LED begins to glow. When the switch is closed, there is no drain current through the FET and therefore the transistor is cut-off and LED does not glow. If the LED glows in both positions, it indicates a shorted FET and if the LED does not glow in either position it indicates an open FET. For a healthy P-channel E-MOSFET, the LED glows when the switch is closed and does not glow when the switch is open.

The P-channel JFETs, P-channel DE-MOSFETs and N-channel E-MOSFETs can be tested by reversing the polarity of the supply voltage and using an NPN transistor instead of a PNP transistor.

5.11 Dual-Gate MOSFET

In a dual-gate MOSFET, an additional second insulated gate is provided as compared to a conventional MOSFET. The flow of current through the MOSFET is controlled by voltages at both the gate terminals. Since the control is exerted by two gates, the dual-gate MOSFET may be considered to be the counterpart of a tetrode. Figure 5.63(a) shows the cross-section of an N-channel dual-gate DE-MOSFET and Figure 5.63(b) shows the circuit symbol. The device acts if two MOSFETs are connected in series. The N+ region in the middle acts as drain for MOSFET-1 and source for the MOSFET-2. The flow of current through the MOSFET is controlled by both gate voltages. For the dual-gate N-channel DE-MOSFET shown in the figure, the drain current decreases when the gate voltage at either of the two gate terminals is made negative. It may be mentioned here that the gate terminal-1 provides higher transconductance as

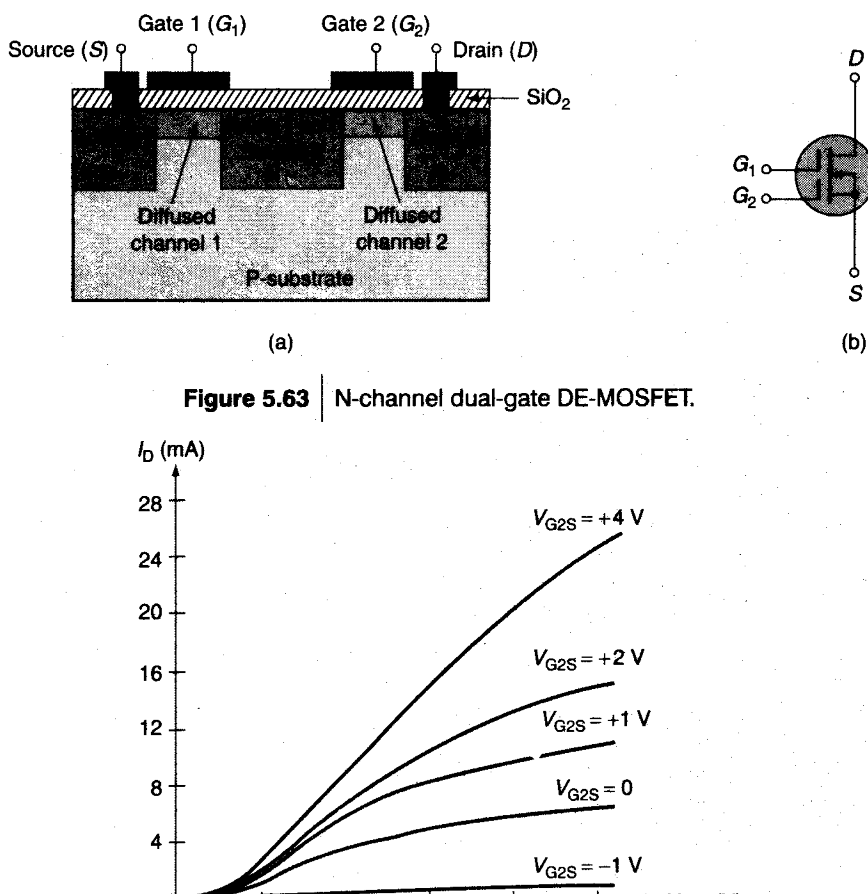


Figure 5.63 | N-channel dual-gate DE-MOSFET.

Figure 5.64 | Transfer characteristics of an N-channel dual-gate DE-MOSFET.

compared to the gate terminal-2. Owing to simultaneous control of two gate voltages, the device is used in applications such as AGC amplifiers, mixers and demodulators. When it is used in an AGC amplifier, the signal to be amplified is connected to Gate-1 and the voltage to control the gain is applied to Gate-2.

Figure 5.64 shows the transfer characteristics of a popular N-channel dual-gate DE-MOSFET. The drain characteristics are similar to that of a conventional N-channel DE-MOSFET.

5.12 VMOS Devices

MOSFETs have smaller power-handling capability as compared to BJTs. The power-handling capability of a MOSFET can be improved if the construction of the MOSFET is modified as shown in Figure 5.65(a). The MOSFET shown in the figure is referred to as vertical metal oxide semiconductor (VMOS) FET or as power MOSFET. VMOS has a vertical structure with the channel formed in the vertical direction rather than the horizontal direction. The operation of a VMOS device is similar to that of an E-MOSFET. No channel exists between drain and source terminals until the gate-source voltage is made positive. For positive values of gate-source voltage, an N-channel is formed close to the gate [Figure 5.65(b)]

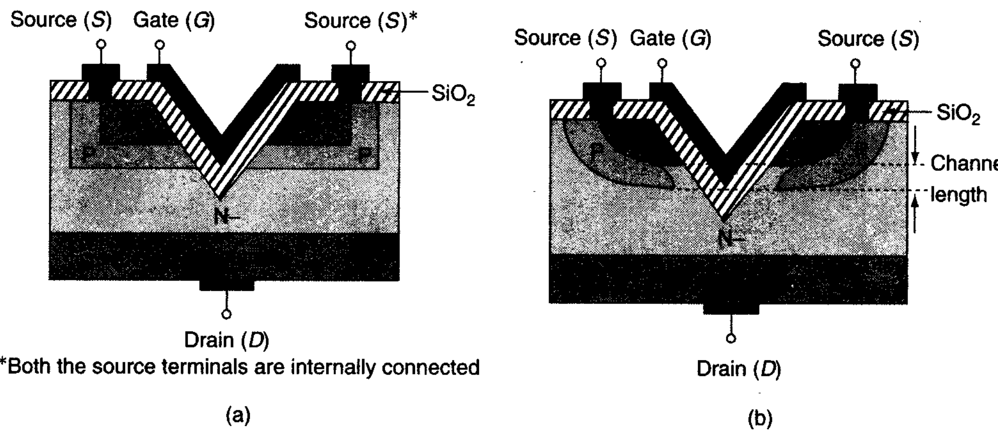


Figure 5.65 (a) Structure of a VMOS device; (b) operation of a VMOS device.

similar to that formed in the case of an E-MOSFET. However, as mentioned above, the channel is formed in the vertical direction. This lets the current carriers to flow between the source and the drain terminals. In the absence of gate-source voltage or for negative values of gate-source voltages, no channel exists and the drain current is zero. Drain and transfer characteristics are the same as shown in the case of planar E-MOSFETs. The MOSFETs discussed earlier are also referred to as planar MOSFETs.

VMOS devices have smaller channel lengths and larger contact area between the channel and the N+ doped regions as compared to MOSFETs, resulting in reduced resistance levels and hence in reduced power-dissipation levels. Also there are two conductive paths from the drain to the source which also leads to higher current rating. Another advantage of VMOS devices is that they have positive temperature coefficient which reduces the possibility of thermal runaway. Also VMOS devices have faster switching times as compared to that of planar MOSFETs as they have reduced charge storage levels.

5.13 CMOS Devices

Complementary metal oxide semiconductor (CMOS) are those semiconductor devices in which both P-type and N-type E-MOSFETs are diffused onto the same chip. The CMOS configuration has extensive applications in computer logic design. CMOS devices offer high input impedance, low power consumption and require far less space as compared to BJT-based logic circuit. However, they offer slower switching speed as compared to BJTs.

Figure 5.66 shows the basic inverter circuit using CMOS configuration. Inverter is a logic circuit that inverts the applied input signal, that is, logic LOW and logic HIGH levels applied at the input terminals result in logic HIGH and logic LOW levels at the output terminals, respectively. The complementary N-type and P-type E-MOSFETs are connected in series, with their gate terminals tied together to form the input terminal. Also, the drain terminals are connected together to form the output terminal. Source terminal of the P-channel MOSFET (S_2) is connected to voltage V_{SS} (between 5 and 15 V) and the source terminal of the N-channel MOSFET (S_1) is connected to the ground.

Figure 5.67 shows the simplified diagram of the CMOS architecture shown in Figure 5.66. The circuit operates as follows: When the input voltage V_{in} is at logic LOW, the gate-source voltage (V_{G2S2}) of the P-channel E-MOSFET is equal to $-V_{SS}$ and the MOSFET is in the ON-state, providing a low resistance path between V_{SS} and the output terminal. The gate-source voltage (V_{G1S1}) of N-channel E-MOSFET is 0 V and therefore it is OFF, resulting in very high impedance between the output terminal and the ground. Therefore, the output voltage V_{out} is equal to the supply voltage V_{SS} or in other words the output voltage (V_{out}) is at logic HIGH.

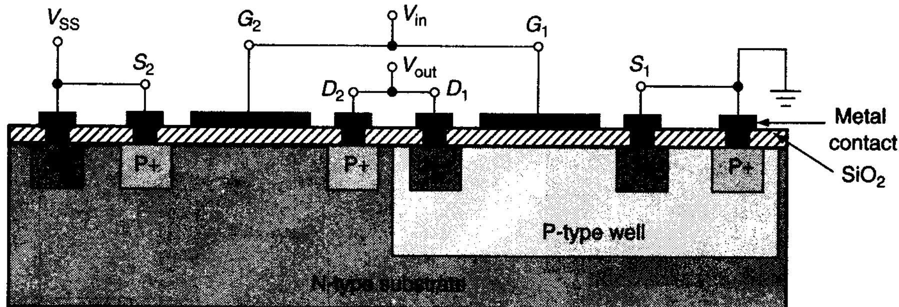


Figure 5.66 | CMOS inverter.

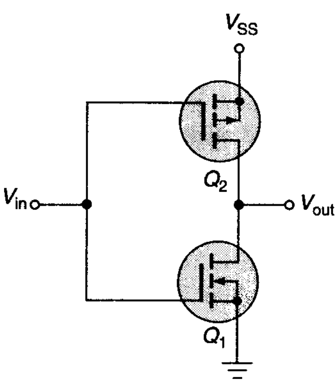


Figure 5.67 | Simplified diagram of CMOS inverter.

When the input voltage V_{in} is at logic HIGH, that is, equal to the supply voltage V_{SS}, the gate-source voltage (V_{G2S2}) of the P-channel E-MOSFET is 0 V and therefore, the MOSFET is in the OFF-state. The gate-source voltage (V_{G1S1}) of the N-channel E-MOSFET is equal to the supply voltage (V_{SS}) and hence it is switched ON, offering a low resistance path. The two MOSFETs form a voltage divider and the output voltage V_{out} is approximately equal to 0 V. Therefore, logic HIGH at the input results in logic LOW at the output. In either state, one of the MOSFETs is OFF. This results in very low power dissipation in the device. Special handling precautions mentioned for MOSFETs are also applicable to CMOS devices.

5.14 Insulated Gate Bipolar Transistors (IGBTs)

IGBTs are three-terminal power semiconductor devices having positive attributes of both BJTs and MOSFETs. IGBTs offer fast switching times similar to that of MOSFETs and lower ON-state voltages and larger blocking voltages similar to that of BJTs. They are used in high efficiency and fast switching applications like switch mode power supplies, traction motor control and induction heating.

Figure 5.68 shows the cross-sectional view of an N-channel IGBT device. We can see from the figure that the construction of IGBT is very similar to that of a VMOS device except that the N+ drain is replaced by P+ collector layer, thus forming a vertical PNP transistor. Figure 5.69 shows the simplified equivalent circuit for the N-channel IGBT. The equivalent circuit shows an N-channel power MOSFET driving a wide base PNP transistor in a Darlington configuration.

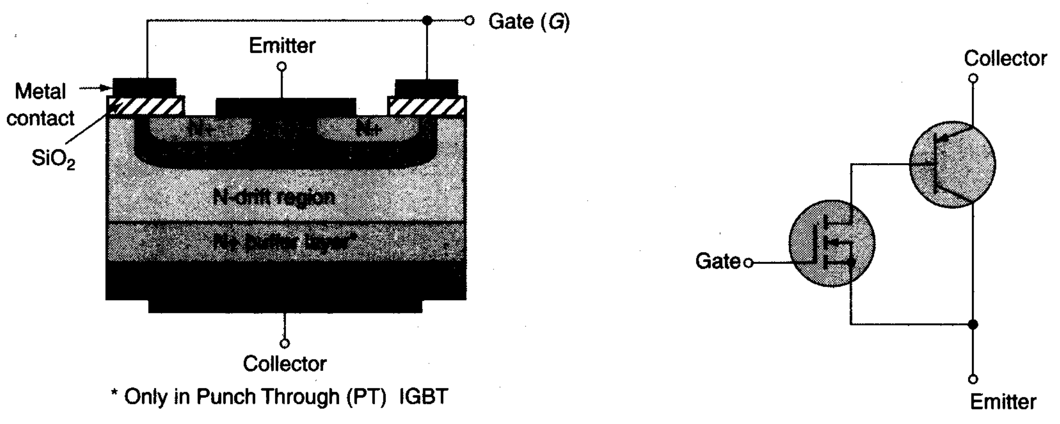


Figure 5.68 | Cross-section of N-channel IGBT.

Figure 5.69 | Simplified equivalent circuit of an N-channel IGBT.

The ON/OFF-state of the device is controlled by the applied gate voltage w.r.t. to the emitter voltage. If the gate-emitter voltage is less that the threshold voltage (V_{TH}) of the MOSFET, no inversion layer is created and the device is in the OFF-state. When the gate-emitter voltage is above the threshold voltage (V_{TH}), enough electrons will be drawn towards the gate to form a conductive channel across the body region, leading to the flow of current between the collector and the emitter terminals.

Figure 5.70 shows the typical output characteristics of an N-channel IGBT device. The output characteristics are quite similar to that of an N-channel E-MOSFET. A noteworthy feature on the IGBT characteristics is the offset of approximately 0.7 V from the origin and the steep slope of the rising portion of the characteristics. The offset is because the ON-state voltage across the IGBT is one diode-drop higher than that of N-channel E-MOSFET. The steep slope of the transfer characteristics is attributed to the fact that current flow in an IGBT is due to flow of both electrons and holes as compared to an N-channel MOSFET where the current flow is due to the flow of electrons only. This reduces the effective resistance to current flow in the drift region. The resulting reduction in the ON-state voltage is the main advantage of IGBTs over power MOSFETs.

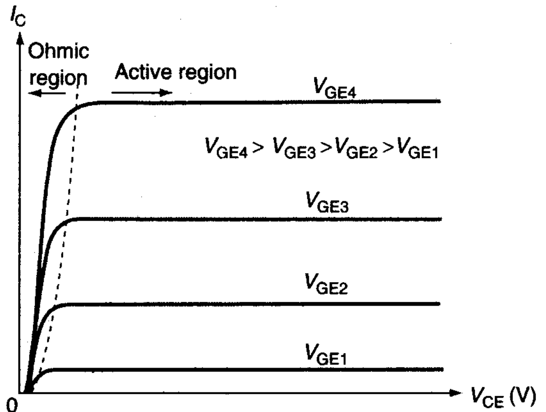


Figure 5.70 | Output characteristics of an N-channel IGBT.

However, IGBTs offer slow switching speeds especially during turn-off. Turn-off in the case of IGBTs is done by reducing the gate-emitter voltage below the threshold voltage. The electron flow in the IGBT as in an N-channel MOSFET stops abruptly. However, in an IGBT holes are left in the drift region and they can only be removed by the process of recombination or by applying a voltage gradient. This results in a tail current in IGBTs during turn-off till all the holes are removed. An N+ buffer layer is added in some IGBTs to control the rate of recombination of holes by absorbing trapped holes during turn-off. IGBTs with N+ buffer layer are called punch-through (PT) IGBTs and those without the N+ buffer layer are called non-punch-through (NPT) IGBTs. PT IGBTs are also referred to as asymmetrical IGBTs and NPT IGBTs as symmetrical IGBTs.

Another problem associated with IGBTs is the occurrence of latch-up phenomenon. Latch-up refers to the failure mode where the IGBT can no longer be turned off by the gate voltage. Latch-up can be explained with the help of a more detailed equivalent circuit of the IGBT as shown in Figure 5.71. The basic structure of an IGBT resembles a thyristor (series of PNPN junctions) and latch-up can occur if the IGBT were not properly used.

Like MOSFETs, IGBTs also are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Therefore similar precautions must be taken while handling IGBTs as taken in the case of MOSFETs.

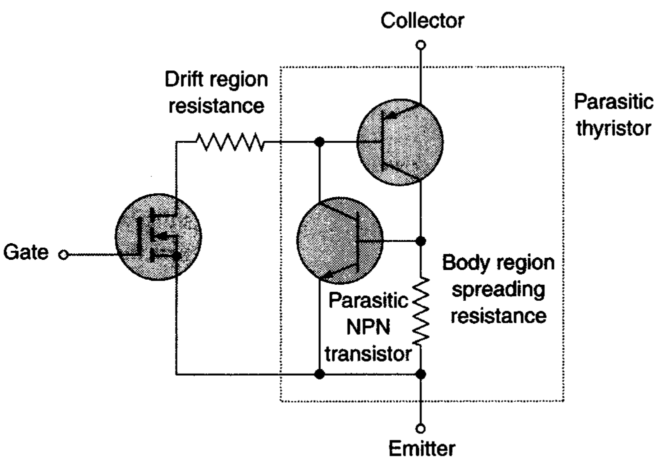


Figure 5.71 | Detailed equivalent circuit of an N-channel IGBT.

KEY TERMS

Amplification factor (μ)
Common-drain configuration
Common-gate configuration
Complementary metal oxide semiconductor (CMOS)
Depletion MOSFET
Dual-gate MOSFET
Dynamic drain resistance (r_d)
Enhancement MOSFET
Field effect transistor (FET)
Fixed-bias configuration
Insulated gate bipolar transistor (IGBT)
Junction field effect transistor (JFET)
Metal oxide field effect transistor (MOSFET)
Shockley's equation
Self-bias configuration
Static drain resistance
Transconductance (g_m)
Vertical metal oxide semiconductor (VMOS)
Voltage-divider configuration

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. FETs are
   a. voltage controlled devices with high input impedance.
   b. current controlled devices with low input impedance.
   c. voltage controlled devices with low input impedance.
   d. current controlled devices with high input impedance.

2. For low values of drain-source voltages, the JFET acts as a
   a. current source.
   b. voltage source.
   c. BJT.
   d. resistor.

3. JFETs are also referred to as square-law devices because
   a. the drain current varies as square of the drain-source voltage for fixed value of gate-source voltage.
   b. the drain current varies as square of the gate-source voltage for fixed drain-source voltage.
   c. the gate current varies as square of the drain-source voltage for fixed value of gate-source voltage.
   d. the gate current varies as square of the gate-source voltage for fixed drain-source voltage.

4. Which of the following devices has revolutionized the field of computers?
   a. BJTs
   b. enhancement MOSFETs
   c. depletion MOSFETs
   d. JFETs

5. Which of the following statements is/are false?
   a. Noise level of an FET device is more than that of a BJT.
   b. Noise level of an FET device is less than that of a BJT.
   c. Input impedance of a MOSFET is greater than that of a JFET.
   d. Input impedance of a MOSFET is less than that of a JFET.
   e. Both (a) and (c).
   f. Both (b) and (c).

6. The transconductance curve of a JFET is
   a. parabolic.
   b. linear.
   c. hyperbolic.
   d. none of the above.

7. Depletion MOSFETs can operate in
   a. depletion mode only.
   b. enhancement mode only.
   c. both depletion and enhancement modes.
   d. none of the above.

8. Dual-gate MOSFETs can be considered to be counterpart of
   a. triodes.
   b. diodes.
   c. tetrodes.
   d. pentodes.

9. The principle of operation of a VMOS device is similar to that of
   a. enhancement MOSFET.
   b. depletion MOSFET.
   c. insulated gate bipolar transistor.
   d. junction FET.

10. Which of the following statements is/are true?
    a. IGBTs offer fast switching times similar to that of MOSFETs and lower ON-state voltages and larger blocking voltages similar to that of BJTs.

b. IGBTs offer fast switching times similar to that of BJTs and lower-ON-state voltages and larger blocking voltages similar to that of BJTs.

c. The equivalent circuit of an IGBT is an N-channel power MOSFET driving a wide base PNP transistor in a Darlington configuration.

d. The equivalent circuit of an IGBT is an N-channel power MOSFET driving a wide base NPN transistor in a Darlington configuration.

e. Both (a) and (c).

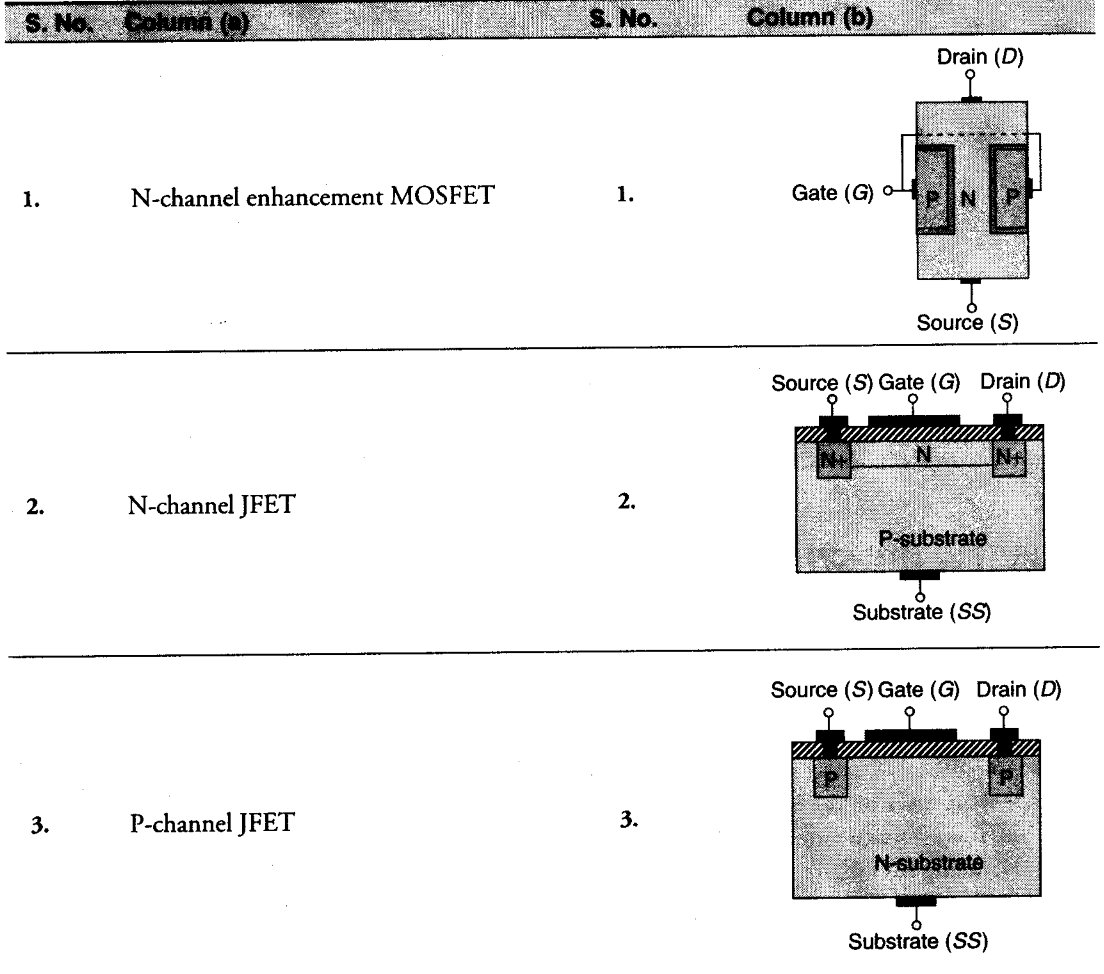
f. Both (a) and (d).

g. Both (b) and (c).

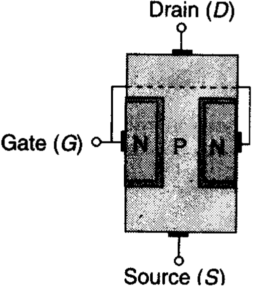
h. Both (b) and (d)

Match the Following

Match the terms in column (a) to those in column (b).



S. No.	Column (a)	S. No.	Column (b)
1.	N-channel enhancement MOSFET	1.	
2.	N-channel JFET	2.	
3.	P-channel JFET	3.	

<table>
<tr><td>4.</td><td>N-channel depletion MOSFET</td><td>4.</td><td>Source (S) Gate (G) Drain (D)
N
N
P-substrate
Substrate (SS)</td></tr>
<tr><td>5.</td><td>P-channel enhancement MOSFET</td><td>5.</td><td>
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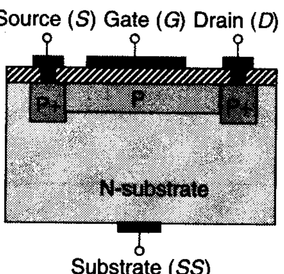
<tr><td>6.</td><td>P-channel depletion MOSFET</td><td>6.</td><td>
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REVIEW QUESTIONS

1. Draw the cross-sectional view of an N-channel JFET and explain its principle of operation. Draw the I_D versus V_{DS} graph for different values of V_{GS} and highlight the different regions of operation.

2. Write short notes on the following:
   a. FET as a voltage variable resistance
   b. Handling MOSFETs
   c. Differences between VMOS and MOSFET
   d. Comparison between BJTs, JFETs and MOSFETs

3. What is an insulated gate bipolar transistor (IGBT)? Is there any difference between IGBT and MOSFET? If yes, then mention any two differences between the two devices.

4. With the help of transfer characteristics for depletion-type and enhancement-type MOSFETs, briefly describe as to how the depletion-type MOSFETs are usually ON devices that can be switched OFF with an appropriate gate signal and the enhancement-type MOSFETs are usually OFF devices that can be switched ON with an appropriate gate signal.

5. With the help of neat diagrams, describe the operation of N-channel depletion and enhancement MOSFETs.
6. Why are FETs known as unipolar devices?
7. Draw the circuit for the voltage-divider configuration using enhancement MOSFETs. Also derive the expression for the operating point.
8. How can one identify the terminals and the type of a MOSFET using laboratory equipments?
9. Explain the principle of operation of a dual-gate MOSFET? Also mention any two of its typical application areas.
10. What are CMOS devices? Explain with the help of relevant diagrams the operation of a CMOS NAND gate.

PROBLEMS

1. An experimental setup using a JFET gave the following readings:
   i. With $V_{GS} = 0$ V and $V_{DS} = 15$ V, $I_D = 15$ mA
   ii. With $V_{GS} = 0$ V and $V_{DS} = 10$ V, $I_D = 14$ mA
   iii. With $V_{GS} = -1$ V and $V_{DS} = 15$ V, $I_D = 13$ mA

   Determine the values of
   a. Drain resistance
   b. Transconductance
   c. Amplification factor
   d. Type of JFET
2. For the circuit shown in Figure 5.72 if the saturation drain current is 5 mA and the pinch-off voltage of the JFET is −4 V, determine the value of quiescent drain current and drain-source voltage. Also determine the value of quiescent gate-source voltage.

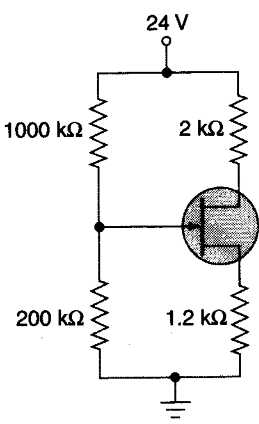


Figure 5.72 | Problem 2.

3. For the AGC circuit shown in Figure 5.73 given that r_o is the drain resistance at $V_{GS} = 0$ V, derive the expression for the voltage gain. Assume that $V_C^2 >> V_P^2$.

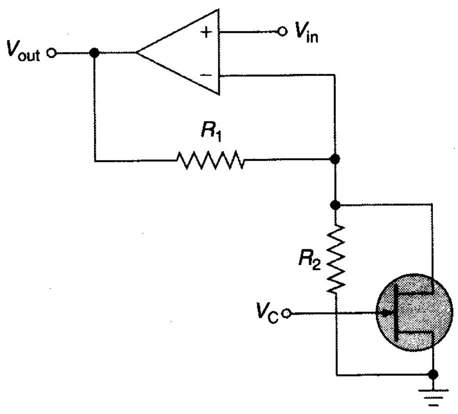


Figure 5.73 | Problem 3.

4. Identify the circuit shown in Figure 5.74. What is the value of current I_{out}?

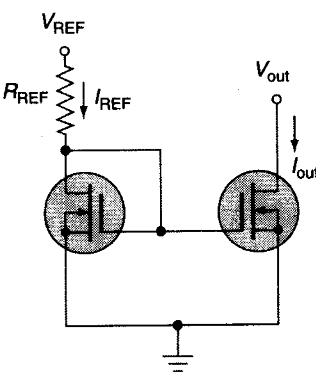


Figure 5.74 | Problem 4.

5. Refer to the circuit shown in Figure 5.75. Given that the transistor β is 100, $V_{BE} = 0.7$ V, saturation drain current of JFET is 10 mA and the pinch-off voltage is –5 V, determine the values of voltages V_D and V_E.

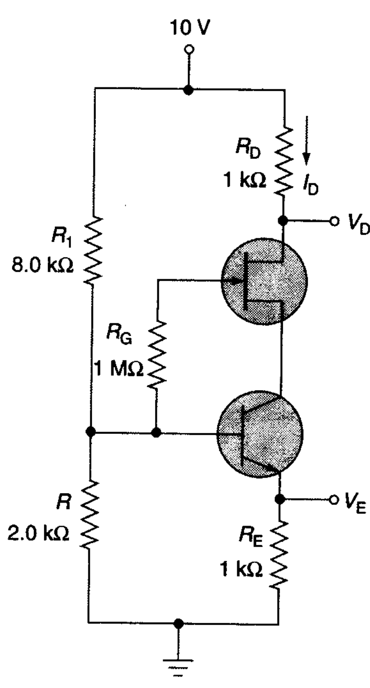


Figure 5.75 | Problem 5.

ANSWERS

Multiple-Choice Questions

1. (a)
2. (d)
3. (b)
4. (b)
5. (f)
6. (a)
7. (c)
8. (c)
9. (a)
10. (e)

Match the Following

1. 2
2. 1
3. 5
4. 4
5. 3
6. 6

Problems

1. (a) 5 kΩ, (b) 2 mA/V, (c) 10, (d) N-channel JFET
2. $I_{DQ} = 3.75$ mA, $V_{DSQ} = 12$ V and $V_{GSQ} = -0.5$ V
3. $1 + \frac{R_1}{R_2} + \frac{R_2}{r_o} \times \left(1 - \frac{2V_C}{V_P}\right)$
4. The circuit is a current mirror, $I_{out} = I_{REF}$
5. $V_D = 8.7$ V, $V_E = 1.3$ V

CHAPTER 6

UJTs and Thyristors

Learning Objectives

After completing this chapter, you will learn the following:

- Operational fundamentals of a unijunction transistor (UJT).
- Electrical characteristics of a UJT and existence of negative resistance region.
- UJT in relaxation oscillator configuration.
- Programmable unijunction transistor (PUT).
- Thyristor and different devices of thyristor family.
- PNPN diode.
- Silicon-controlled rectifier (SCR).
- DIAC and TRIAC.
- Gate turn-OFF thyristor (GTO).
- Rate effect in thyristors.
- Electrical parameters of thyristors.
- Thyristor applications.

The focus in this chapter is on two very popular current-controllable negative resistance semiconductor devices, that is, thyristors and unijunction transistors (UJTs). Thyristor is a generalized name for solid-state semiconductor devices having four or more semiconductor layers and three or more semiconductor junctions. These devices can be with or without the gate-control terminal and act like a latching type of switch. PNPN diode is the most basic device in the family of thyristors. Other popular devices in the family include silicon-controlled rectifier (SCR) and its variants like silicon unilateral switch (SUS), silicon bilateral switch (SBS), DIAC and TRIAC. SCR is the most widely used device in the family of thyristors and the term thyristor is used interchangeably with SCR. Other devices discussed in the chapter include gate turn-OFF thyristors and programmable unijunction transistors (PUT). The topics covered in the chapter include operational principle, electrical characteristics, major performance specifications and typical circuit applications of these devices.

6.1 Unijunction Transistor

Unijunction transistor commonly known as UJT is a semiconductor device with one PN junction as is evident from the word unijunction in its name. Since it has got three terminals like a transistor, it is called unijunction transistor. 2N 2646 is the most commonly used UJT type number.

Construction

Figures 6.1(a) and (b), respectively, show the constructional features and circuit symbol of a UJT. As shown in Figure 6.1(a), it comprises a lightly doped N-type silicon bar with two ohmic contacts called base terminals, B_1 and B_2, made to its two extreme ends and P-type emitter placed closer to the base B_2 to form a PN junction. Figure 6.2 shows the electrical equivalent circuit of a UJT. The equivalent circuit comprises a potential divider arrangement of two resistors and a PN junction diode. Resistor R_{BB1} represents the resistance of base bar between B_1 terminal and the PN junction and resistor R_{BB2} represents resistance of the base bar between B_2 terminal and the PN junction. R_{BB1} has been shown as a variable resistance as its value depends upon the emitter current flowing through the PN junction when it is forward-biased. For $I_E = 0$, total resistance of the base bar ($= R_{BB1} + R_{BB2}$) is termed as R_{BB}. R_{BB} lies in the range of 4–10 kΩ. Another parameter defined for a UJT is the intrinsic stand-off ratio η equal to $[R_{BB1}/(R_{BB1} + R_{BB2})]$ with value of R_{BB1} taken at $I_E = 0$. η is in the range of 0.5–0.8 and is typically 0.7, which also signifies that the emitter terminal is closer to B_2 terminal.

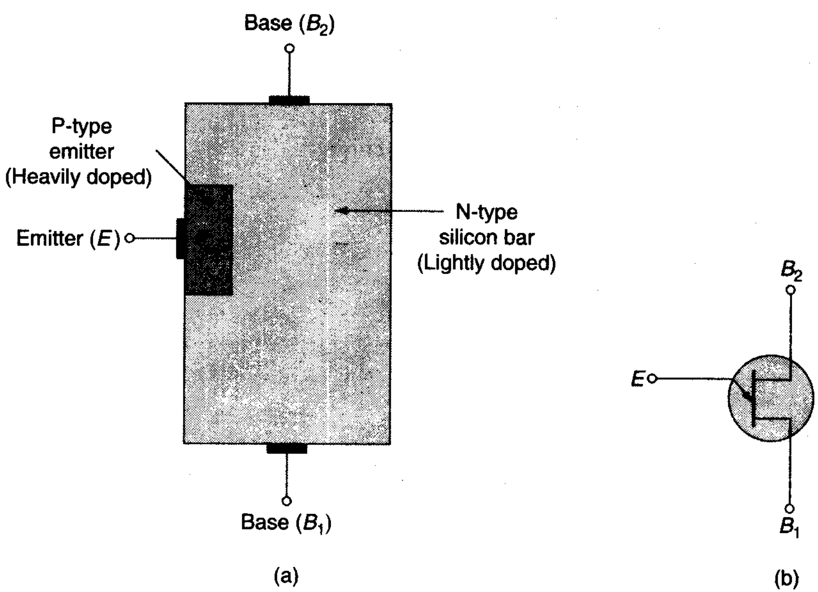


Figure 6.1 Unijunction transistor: (a) Construction; (b) circuit symbol.

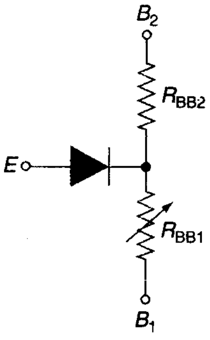


Figure 6.2 Electrical equivalent circuit of UJT.

Operational Principle

The operational principle of a UJT can be best explained with the help of its electrical characteristics or to be more precise its input V–I characteristics. Figure 6.3 shows the electrical circuit for determining the input characteristics. During operation, B_2 terminal is made more positive with respect to B_1 terminal. Also, it is essential to forward bias the PN junction diode by a voltage equal to its cut-in voltage V_γ, which is in the range of 0.35–0.7 V for any significant emitter current I_E to flow through the PN junction. In the absence of the required forward bias, voltage across R_{BB1} is given by ηV_{BB}. Therefore, if the PN junction were to be forward-biased, the externally applied voltage to the emitter terminal must at least be equal to the sum of ηV_{BB} and the cut-in voltage of the diode junction. It is expressed by Eq. (6.1). The emitter voltage V_E at which diode starts conducting is termed as V_P.

$$V_P = \eta V_{BB} + V_\gamma \tag{6.1}$$

As the emitter voltage V_E is increased, initially the current remains negligibly small in magnitude until a voltage (= V_P) is reached at which the diode is forward-biased. After that current increases rapidly. It is seen that as the current increases, the voltage decreases giving a negative resistance region. Such behavior can be explained by considering the fact that due to increase in forward current, the resistance of $E - B_1$ region falls rapidly resulting in reduction in the voltage. Finally when I_E becomes very large, it may be considered to be much greater than I_{B2}. Under these conditions, the curve approaches asymptotically the curve for $I_{B2} = 0$ giving rise to a valley point. The curve for $I_{B2} = 0$ is the same as it would be for ordinary PN junction diode. Figure 6.4 shows V_E–I_E characteristics.

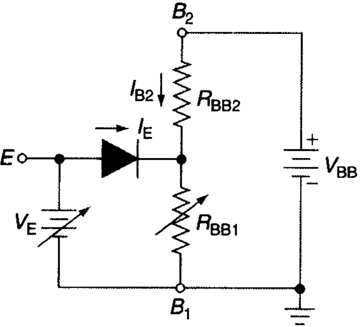


Figure 6.3 | Electrical circuit for determining input characteristics of UJT.

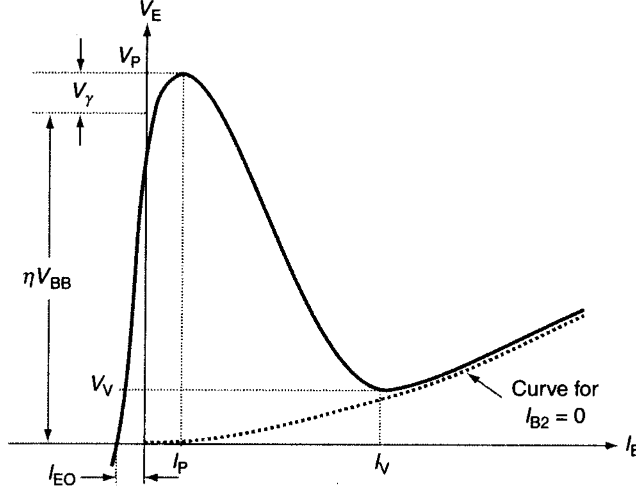


Figure 6.4 | V_E–I_E characteristics of UJT.

The region before the peak point (V_P, I_P) is called cut-off region as the input diode remains reverse-biased in this region. The region after the valley point (V_V, I_V) is termed as saturation region as there is not much increase in the emitter voltage for large changes in emitter current.

Current-Controllable Device

As is seen from the V–I characteristics, the curve is a single-valued function of current and a multi-valued function of voltage. A single-valued function of current implies that for each current value, there is a unique voltage. Such a behavior is contrary to the one observed in the case of tunnel diode, which could be expressed by a single-valued function of voltage. That is what made tunnel diode a voltage-controllable device. Owing to single-valued function of current nature of its V–I characteristics, a UJT is called a current-controllable device.

UJT Relaxation Oscillator Circuit

Figure 6.5(a) shows the basic UJT-based relaxation oscillator circuit. The waveform that appears across the capacitor is shown in Figure 6.5(b). Initially UJT is in the cut-off region. That is, the input diode is reverse-biased. The capacitor starts charging from $+V$ through R. When the voltage V_{out} across the capacitor becomes large enough to forward bias the input diode, the capacitor starts discharging through the low resistance between the emitter–base B_1 region and resistor R_1. This discharge process continues until it reaches a point where input diode is again reverse-biased. At this point, the capacitor starts charging again. The process of charging through R, which is comparatively a higher resistance, and discharging through low forward resistance of input diode and R_1 continues and gives rise to a waveform as shown in Figure 6.5(b). The frequency of oscillation is given by

$$f = \frac{1}{RC \times \ln\{1/(1-\eta)\}} \tag{6.2}$$

If the capacitor in the relaxation oscillator of Figure 6.5(a) could be charged through a constant current source as shown in Figure 6.6(a), the result will be a perfect sawtooth waveform [Figure 6.6(b)].

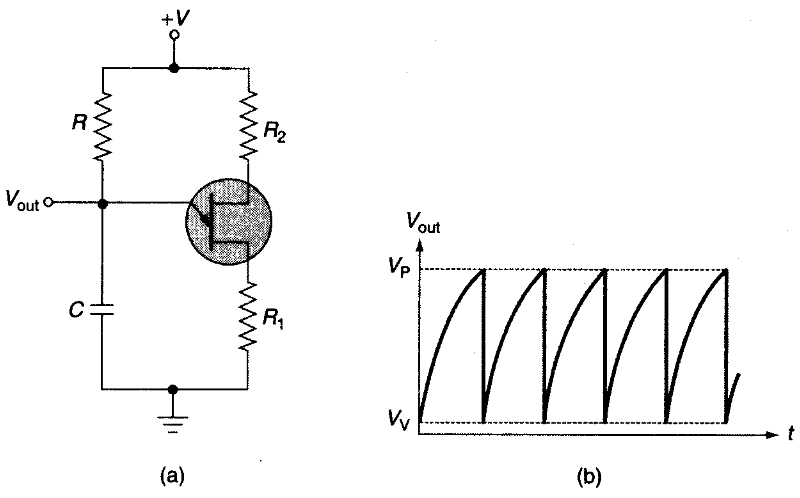


Figure 6.5 | UJT-based relaxation oscillator circuit.

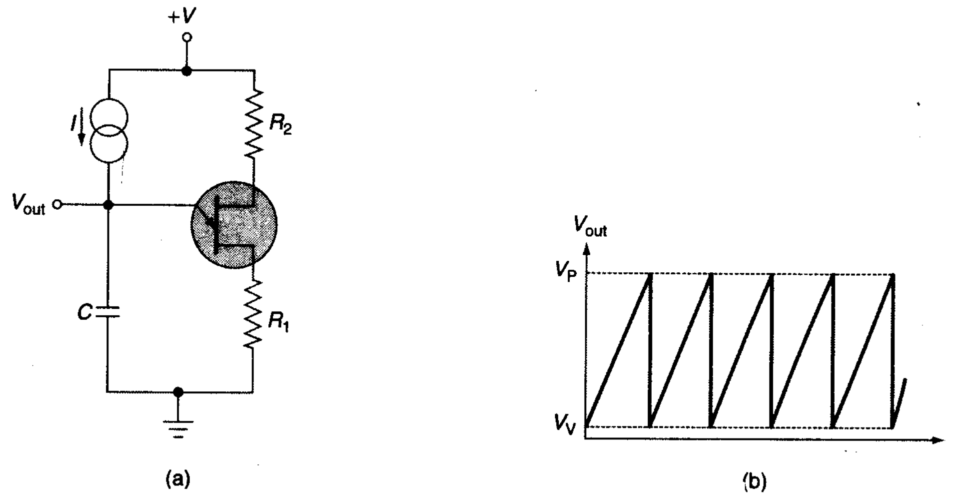


Figure 6.6 | Constant current charging in UJT relaxation circuit.

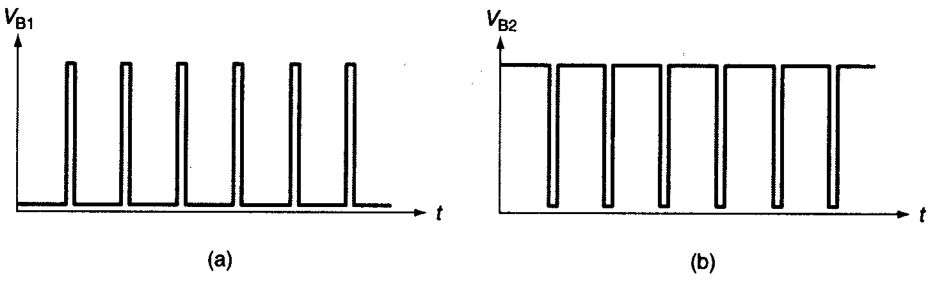


Figure 6.7 | (a) Waveforms at B_1 terminal; (b) waveforms at B_2 terminal.

If we see the voltage waveforms at B_1 and B_2 terminals, it is observed that we get a train of positive pulses at B_1 and a train of negative pulses at B_2. The pulses occur during the time UJT is ON. The waveforms are shown in Figures 6.7(a) and (b).

It may be mentioned here that UJT is no longer a popular device for building oscillators. It has been largely replaced by opamp and timer IC-based circuits.

EXAMPLE 6.1 *Refer to the UJT-based relaxation oscillator circuit of Figure 6.8(a). The waveform observed across capacitor C is shown in Figure 6.8(b). Determine the intrinsic stand-off ratio η of the UJT used in the circuit. Also determine the time period T of the waveform. (Given that the forward-biased diode voltage drop = 0.7 V.)*

Solution

1. From the waveform shown in Figure 6.8(b), peak voltage $V_P = 7.9$ V.
2. Also, $V_P = \eta \times V + V_D$, where $V = 12$ V and V_D is the forward-biased diode voltage drop = 0.7 V.

3. Substituting for V_P, V and V_D, we get the value of η as

$$\eta = (V_P - V_D)/V = (7.9 - 0.7)/12 = 0.6$$

4. Intrinsic stand-off ratio, $\eta = 0.6$.
6. Time period T is given by $RC \times \ln[1/(1-\eta)] = 10 \times 10^3 \times 0.1 \times 10^{-6} \times \ln[1/(1-0.6)] = 0.001 \times \ln 2.5 = 0.92$ ms.

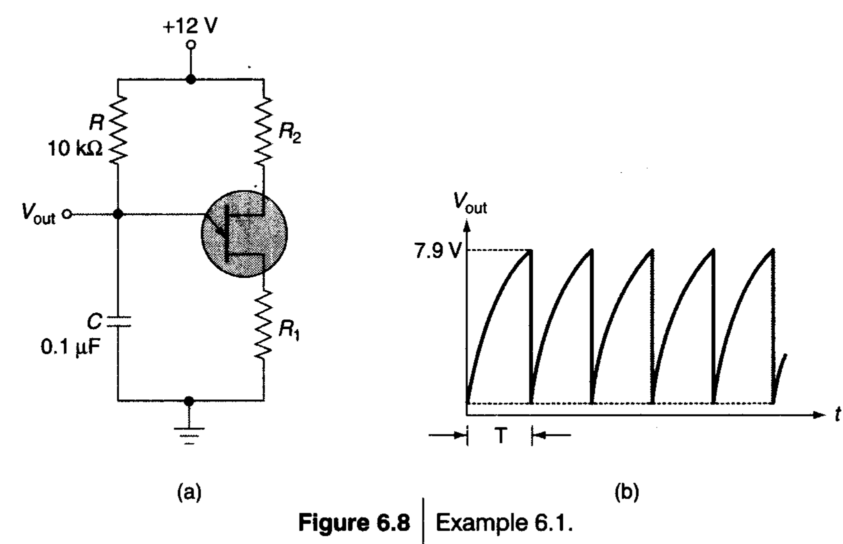


Figure 6.8 | Example 6.1.

6.2 PNPN Diode

It is a four-layer diode consisting of four alternate layers of P-type and N-type materials as shown in Figure 6.9(a). The P-type and N-type semiconductor regions on the extreme are called anode and cathode, respectively. Figure 6.9(b) shows the circuit symbol of the PNPN diode. The PNPN diode is also referred to as a Shockley diode. A device very similar to a PNPN diode is the silicon unilateral switch (SUS), except that its forward voltage drop after firing is higher than the PNPN diode.

If anode (P-type) is made positive with respect to the cathode (N-type), junctions J_1 and J_3 are forward-biased. This applied voltage then effectively appears across junction J_2, thus reverse biasing junction J_2. Now if the applied voltage is increased, a stage comes when the semiconductor junction J_2 breaks down. We have

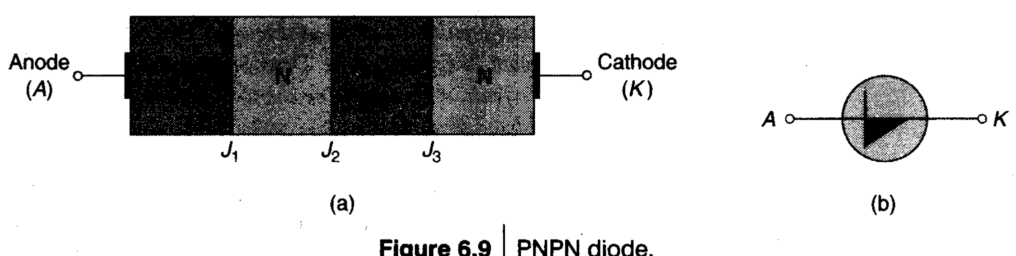


Figure 6.9 | PNPN diode.

studied earlier in Chapter 2 that the breakdown of PN junction occurs when the reverse voltage applied to it exceeds the peak inverse voltage of the diode.

At this breakdown voltage, the current increases all of a sudden from a very small value to a very large value. This increase in current is accompanied by reduction in the voltage giving rise to a negative resistance region. At this point, referred to as break-over point, the PNPN diode switches from its OFF-state (blocking state) to its ON-state.

Operation of a PNPN diode can also be explained by considering it as back-to-back connected NPN and PNP bipolar transistors as shown in Figure 6.10. However, it may be mentioned here that two transistors connected back-to-back do not make a PNPN diode.

The collector current of a bipolar transistor in the active region is given by

$$I_C = -\alpha I_E + I_{CO} \tag{6.3}$$

where I_C is the collector current leaving the transistor; I_E is the emitter current entering the transistor; α the short-circuit gain of CB configuration; I_{CO} the reverse saturation current.

Note that both the transistors will be in active region because the collector junctions of both of them (i.e., J_2) are reverse-biased and their emitter junctions (J_1 of PNP transistor and J_3 of NPN transistor) are forward-biased.

$$I_{E1} = \text{Emitter current of } Q_1 = +I \text{ and } I_{E2} = \text{Emitter current of } Q_2 = -I$$

Also the leakage current for Q_1 (I_{CO1}) is negative and for Q_2 (I_{CO2}) is positive. Let I_{CO} be the total leakage current of the device. Therefore

$$I_{CO2} = -I_{CO1} = I_{CO}/2$$

Equation (6.3) can, therefore, be employed to write expressions for collector currents I_{C1} and I_{C2} as Eqs. (6.4) and (6.5), respectively.

$$I_{C1} = -\alpha_1 I + I_{CO1} \tag{6.4}$$

$$I_{C2} = +\alpha_2 I + I_{CO2} \tag{6.5}$$

Now in the case of transistor Q_1, substituting the sum of all currents entering the transistor equal to zero, we get

$$I + I_{C1} - I_{C2} = 0 \tag{6.6}$$

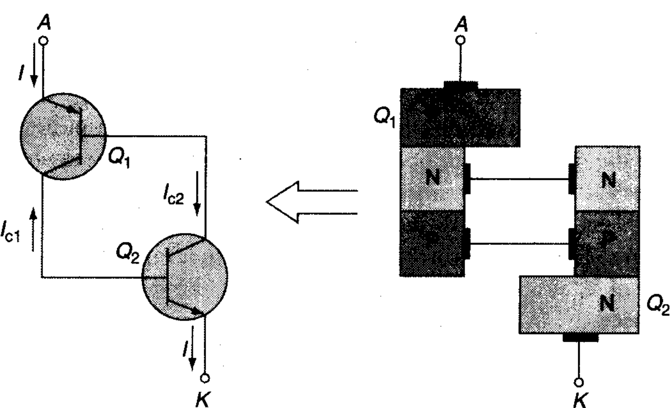


Figure 6.10 PNPN diode represented as back-to-back connected NPN and PNP transistors.

Combining Eqs. (6.4)–(6.6) and putting $I_{CO2} = -I_{CO1} = I_{CO}/2$, expression for current I can be written as

$$I = \frac{I_{CO2} - I_{CO1}}{1-(\alpha_1+\alpha_2)} = \frac{I_{CO}}{1-(\alpha_1+\alpha_2)} \tag{6.7}$$

Here α_1 and α_2 are the forward current gains of the two transistors in common-base configuration and will have values lying between 0 and 0.95 depending upon the currents flowing through them. When we are increasing the voltage, effectively we are doing nothing but increasing the value of α_1 and α_2 and when $\alpha_1 + \alpha_2$ reaches unity, there is a sudden increase in anode current as is obvious from Eq. (6.7).

$$I = \frac{I_{CO}}{1-(1)} \quad \text{for } (\alpha_1+\alpha_2) \to 1$$

Please note that if $(\alpha_1 + \alpha_2)$ were to exceed unity, direction of current would not have reversed as is indicated by Eq. (6.7). The reason for this is as follows. The moment $(\alpha_1 + \alpha_2)$ becomes unity or approaches unity, current becomes exceedingly large. This brings all three junction diodes into saturation region. In other words, Q_1 and Q_2 go to saturation due to their collector junctions being forward-biased. As a consequence of transistors going to saturation, magnitudes of α_1 and α_2 decrease so that $(\alpha_1 + \alpha_2)$ never exceeds unity. Put in another way, transistors Q_1 and Q_2 enter saturation only upto the extent that $(\alpha_1 + \alpha_2)$ remains unity.

PNPN Diode Material

The semiconductor material used for making PNPN diodes is always silicon. Germanium is never used as it does not have a stable OFF-state. To elaborate it further, with germanium as the semiconductor material, the magnitudes of α may become large enough to give $(\alpha_1 + \alpha_2)$ equal to unity for a very small value of applied voltage thus leading to an unstable OFF-state.

PNPN Diode Characteristics

The V–I characteristics of a PNPN diode are shown in Figure 6.11. The characteristic curve can be divided into three regions, namely, cut-off region also known as forward-blocking state, saturation region and the transition region shown as the dotted line. In the cut-off region, current through the device is ideally zero and practically extremely small, equal to the current that would flow through a reverse-biased PN junction. This region extends to a voltage equal to the break-over voltage marked V_{BO} in Figure 6.11. As the anode-to-cathode voltage exceeds the break-over voltage, the device switches rapidly from the cut-off region to the saturation region. The dotted line in fact indicates this rapid switching action and also that the device cannot operate in this region. Once the device has broken-over, it stays in that state as long as the current remains above a value called the holding current marked I_H in Figure 6.11. In order to bring the device to the cut-off state, it is imperative to bring the current below the holding current value. The voltage corresponding to the holding current is the holding voltage marked as V_H. The value of V_H is approximately 0.7 V. However, this voltage is a function of the current flowing through the device. It, in fact, increases with the magnitude of current. As an example, for PNPN diode type number 1N5158, the holding voltage increases from 1 V to 2 V as the current increases from 200 mA to 2 A.

A PNPN diode behaves like an ON–OFF switch. The switch is open in the forward-blocking state and is closed in the saturation region. The characteristics of a PNPN diode for a negative anode-to-cathode voltage are similar to that of a reverse-biased diode.

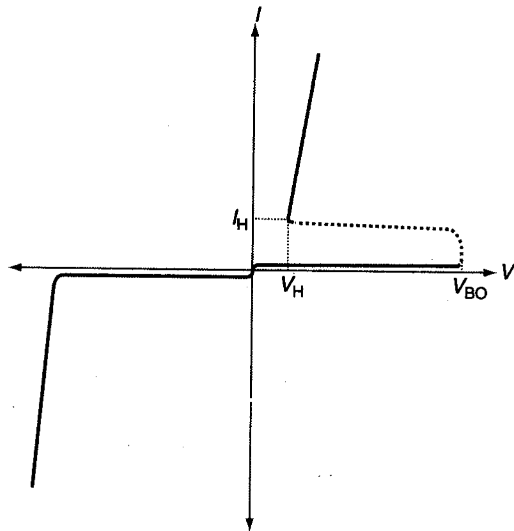


Figure 6.11 | V–I characteristics of PNPN diode.

EXAMPLE 6.2

The PNPN diode used in the circuit of Figure 6.12(a) has a break-over voltage of 20 V and a holding current of 5 mA. The V–I characteristics of the device are shown in Figure 6.12(b). Determine (a) current flowing through the device and (b) the region of operation of the device if the resistance R were increased to 10 kΩ.

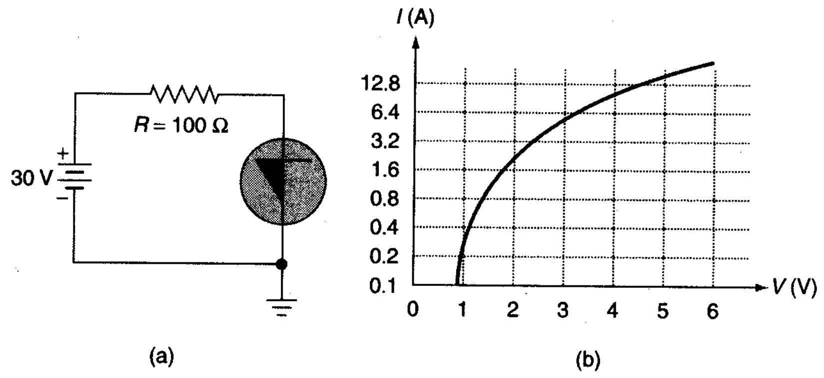


Figure 6.12 | Example 6.2.

Solution

1. The applied voltage is greater than the break-over voltage. The device is therefore in the saturation region. The current flowing through the device to first approximation is given by 30/100 = 0.3 A.
2. For current equal to 0.3 A, the voltage drop across the device as seen from the characteristic curve of Figure 6.12(b) is 1.0 V.

3. Therefore, more exact value of current can be computed from (30 − 1)/100 = 0.29 A.
4. When the resistance R is increased to 10 kΩ, the current through the device reduces to 30/10000 = 3 mA, which is less than the holding current value. Therefore the device switches back to the cut-off state.

EXAMPLE 6.3

Refer to the PNPN diode circuit of Figure 6.13. The break-over voltage and holding current specifications of the device are 12 V and 4 mA, respectively. The variable voltage source is set in such a way that the device is conducting. If the knee voltage of the device is taken to be 0.7 V, determine the applied voltage at which the device will turn OFF.

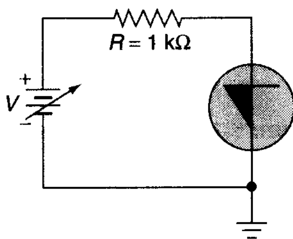


Figure 6.13 | Example 6.3.

Solution

1. The device will turn off when the current falls below the holding current value.
2. If the applied voltage at that point is V, then $(V - 0.7)/1 \times 10^3 = 4 \times 10^{-3}$. That is, $V = 4.7$ V.

PNPN Diode as Relaxation Oscillator

Figure 6.14(a) shows the basic relaxation oscillator circuit configured around a PNPN diode. The circuit functions as follows. Initially the PNPN diode is in the cut-off state and therefore behaves like an open switch. Capacitor C begins to charge exponentially through resistor R towards the applied DC voltage V. As the voltage across the capacitor reaches a value equal to the break-over voltage of the PNPN diode, the device breaks down and rapidly switches to the saturation region of its V–I characteristics. PNPN diode is now in the ON-state and behaves like a closed switch or a near short circuit. The capacitor rapidly (almost instantaneously) discharges through the PNPN diode. The discharge process continues as long as the current through the PNPN diode remains above the holding current value. The moment it falls below that value, the PNPN diode rapidly switches to the OFF-state. The capacitor begins to charge again through R and the process is repeated. Thus, the capacitor repetitively charges and discharges through R and PNPN diode, respectively. The charging time is determined by the product of R and C and charging voltage V. Equation (6.8) represents the charging process (assuming $V_H = 0$).

$$V_c = V \times (1 - e^{-t/RC}) \tag{6.8}$$

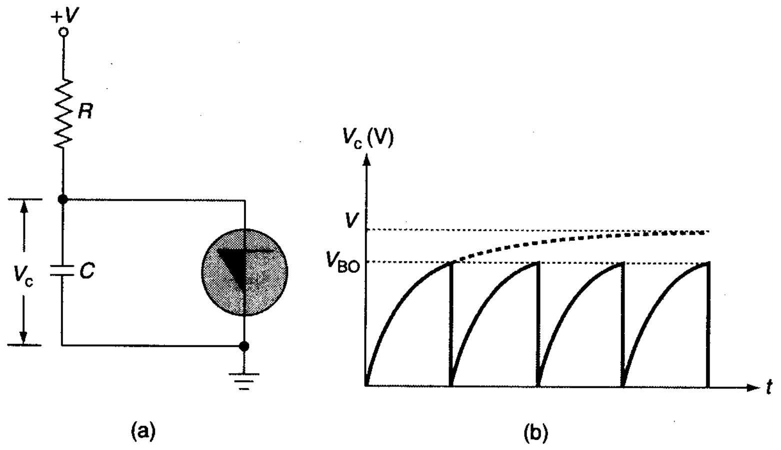


Figure 6.14 | PNPN diode relaxation oscillator.

The discharge time is determined by the product of C and ON-resistance of the PNPN diode. The waveform across the capacitor resembles a sawtooth, more so when the charging voltage V is large as compared to the break-over voltage of the PNPN diode. Figure 6.14(b) shows the waveform. The waveform becomes a perfect sawtooth if resistor R were replaced by a constant current source. The charging process in that case would be represented by

$$V_c = I \times t/C \tag{6.9}$$

where I is the magnitude of the constant charging current.

EXAMPLE 6.4

Refer to the relaxation oscillator circuit of Figure 6.15. The PNPN diode used in the circuit is 1N 5158 having a break-over voltage and holding current specifications of 10 V and 4 mA, respectively. Draw the waveform across the capacitor indicating its timing parameters (assume V_H = 0).

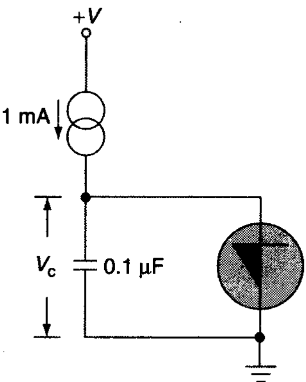


Figure 6.15 | Example 6.4.

Solution

1. The capacitor in this case is being charged from a constant current source of magnitude equal to 1 mA.
2. Therefore, the instantaneous voltage appearing across the capacitor is given by $V_c = (I/C) \times t$. Now $I = 1.0$ mA and $C = 0.1$ μF.
3. Considering that the ON-resistance of the PNPN diode is negligible, the waveform appearing across the capacitor will be a sawtooth waveform as shown in Figure 6.16. The capacitor voltage linearly rises to a voltage equal to the break-over voltage of the device from where it discharges almost instantaneously through the device. The voltage rise is linear due to constant current charging.
4. In the present case, the capacitor voltage rises to 10 V before the device switches to the ON-state.
5. The time period required by the capacitor to charge to 10 V is given by $0.1 \times 10^{-6} \times 10/10^{-3} = 1$ ms.
6. The sawtooth waveform therefore has a time period of 1 ms.

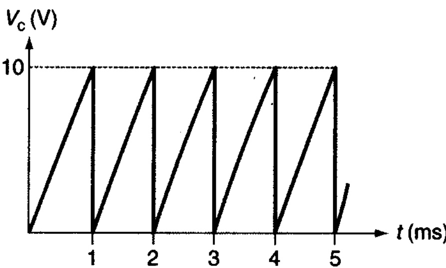


Figure 6.16 | Solution to Example 6.4.

Rate Effect

The effect of rate of change of applied voltage on the break-over voltage is termed as rate effect. When the PNPN diode is in the forward-blocking or OFF-state, the center diode junction J_2 is reverse-biased while the two outermost diode junctions J_1 and J_3 are forward-biased. All reverse-biased diodes have some capacitance across them. A four-layer diode represented by two forward-biased and one reverse-biased diode is shown in Figure 6.17.

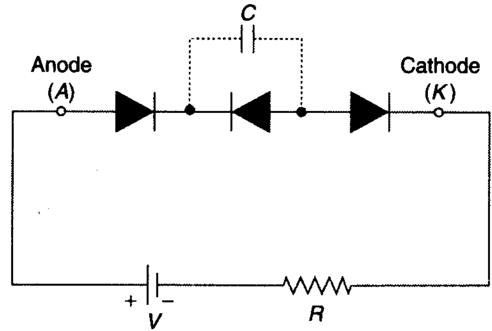


Figure 6.17 | Rate effect in PNPN diodes.

When rate of change of applied voltage is low, capacitance C offers very high reactance with the result that the current through the capacitance can be ignored. When the rate of change of applied voltage is sufficiently large then the current through C, when added to the total current, enables the sum $(\alpha_1 + \alpha_2)$ to reach unity at an applied voltage less than the break-over voltage. In other words, high rate of change of applied voltage effectively reduces the break-over voltage leading to premature firing of the device. This phenomenon is called rate effect.

6.3 Silicon-Controlled Rectifier

The construction of a silicon-controlled rectifier (SCR) is exactly the same as that of a four-layer diode with the only difference that the connection to one of the inner layers adjacent to the cathode layer is brought out to exercise control over the switching characteristics of the device. This control terminal is called the gate-terminal, cathode gate to be more precise. Figure 6.18(a) shows the circuit symbol of an SCR. Considering the PNPN device to be equivalent to back-to-back connection of a PNP and an NPN transistor, we can notice that the gate terminal is nothing but the base terminal of the NPN transistor as shown in Figure 6.18(b).

The control action of the gate terminal in the case of an SCR functions as follows. A momentary pulse applied to the gate terminal increases the base current of the NPN transistor initiating a regenerative feedback action. This regenerative feedback action ultimately drives both the transistors to saturation causing switching-ON action of the device even if the anode-to-cathode voltage were less than the break-over voltage. The anode-to-cathode voltage at which the device can be triggered to the ON-state is a function of the gate trigger current. In other words, magnitude of trigger current required to turn the device ON depends upon the anode-to-cathode voltage. Larger gate current can trigger the device ON for a lower anode-to-cathode voltage.

In the case of SCR, only the cathode gate is available. If the anode gate is also made available, then the device is referred to as the silicon-controlled switch (SCS). In other words, SCS is a four-layer PNPN device where connection to all the four layers are available. The characteristics of the device are essentially the same as those of an SCR. Figure 6.18(c) shows the circuit symbol of SCS.

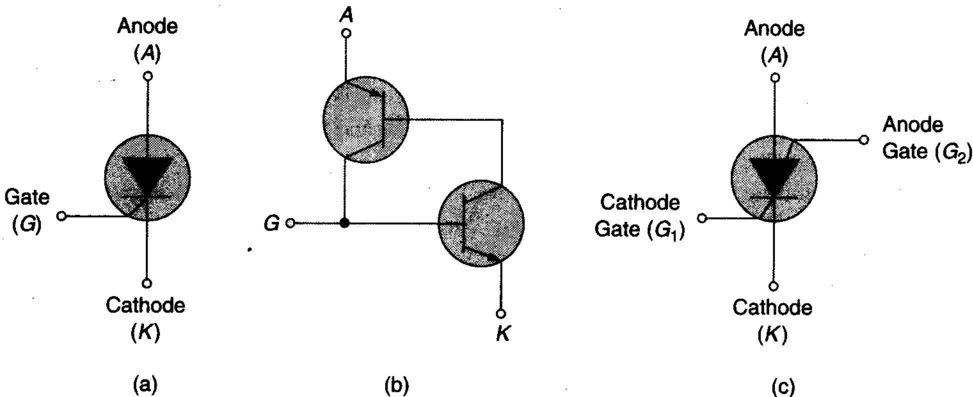


Figure 6.18 (a) Circuit symbol of SCR; (b) equivalent circuit of SCR; (c) circuit symbol of SCS.

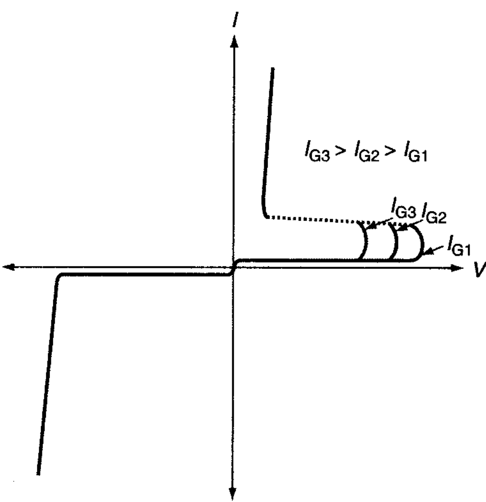


Figure 6.19 | V–I characteristics of an SCR.

V–I Characteristics

V–I characteristics of an SCR are similar to those discussed in the case of a PNPN diode in Section 6.2 (PNPN diode characteristics). However, in the case of SCR, we can plot a family of characteristics in the first quadrant for different values of gate current as shown in Figure 6.19. As is clear from the family of characteristic curves, the break-over voltage reduces with increase in gate trigger current. In other words, as the anode-to-cathode voltage reduces, the magnitude of gate current required to trigger the device to the ON-state increases. The V–I characteristics in the third quadrant are same as that in the case of a PNPN diode. The gate-triggering requirements of an SCR are discussed in the following section.

Gate-Triggering Characteristics

The gate-triggering characteristics of an SCR are a plot of gate voltage (V_G) versus gate current (I_G). As the gate-cathode circuit of an SCR (or a thyristor in general) is nothing but a forward-biased PN junction, the characteristics curve resembles the one for a forward-biased PN junction diode. The gate-trigger voltage (V_{GT}) is the gate-to-cathode voltage required to trigger the device to the ON-state and gate-trigger current (I_{GT}) is the forward-biased current flowing in gate-cathode circuit. We should also remember that the P-and N-type semiconductor materials constituting the gate and cathode regions, respectively, in an SCR are lightly doped.

Owing to light doping, there is a spread in the V–I characteristics even for a given type of SCR. This spread is shown in Figure 6.20 by characteristic curves "1" and "2". In addition, there are minimum and maximum values of gate voltage that can be applied to the device. Similarly there are minimum and maximum values of gate current too. Yet another requirement that needs to be fulfilled is that of the power dissipation. There is always a rated gate power dissipation specified for the SCR which should not be exceeded. This is also shown in Figure 6.20. All these requirements together define the operating area for the gate-trigger circuit. This operating area has been shown shaded in Figure 6.20. The boundary specified by the power dissipation is for the average value of the gate power dissipation. A relatively higher dissipation may be permitted for shorter pulse durations. For example, SCR type number

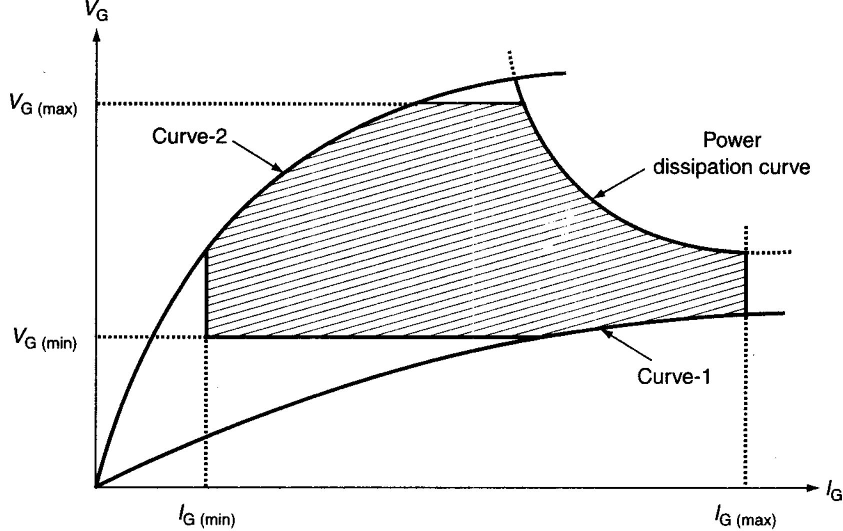


Figure 6.20 | Gate-triggering characteristics.

2N 3668 has P_G(av) rating of 0.5 W and a transient gate power dissipation P_{GM} specification of 40 W for a trigger pulse duration of 10 μs. Now such a device could be triggered by a continuous current of 200 mA at a trigger voltage of 2.5 V. It could also be triggered by a 2 A trigger pulse at 20 V provided that trigger pulse was no wider than 10 μs.

Higher gate-trigger currents yield faster turn-on. But the fast turn-on of the SCR is also not without problems. If the rate of rise of the ON-state current (di/dt) exceeds the critical value of di/dt, the device could get damaged due to creation of localized hot spots. The gate-triggering characteristics vary with temperature. At lower temperatures, one requires higher gate-trigger voltage and current. For example, for SCR type number 2N 3668, the maximum values of V_{GT} and I_{GT} are 2 V and 40 mA, respectively, at a junction temperature of 25°C. At –40°C, these are specified as 3 V and 80 mA, respectively. At 100°C, the values are about 1.5 V and 30 mA. It may be mentioned here that the above discussion is valid for all devices of the thyristor family with gate control.

6.4 DIAC and TRIAC

A DIAC is a bi-directional thyristor. It can be considered to be equivalent to two PNPN devices connected back-to-back [Figure 6.21(a)]. Figure 6.21(b) shows the circuit symbol. As we can see from the figure, it is a two-terminal device with the terminals designated as Main Terminal-1 (MT-1) and Main Terminal-2 (MT-2). The V–I characteristics of a DIAC are similar to those of a four-layer PNPN diode with the difference that a DIAC exhibits identical characteristics both in the forward (first quadrant) and reverse (third quadrant) directions [Figure 6.21(c)].

A TRIAC is equivalent to a DIAC with the gate contact. It is a three-terminal device and the terminals are designated as Main Terminal-1 (MT-1), Main Terminal-2 (MT-2) and Gate (G). Figure 6.22 shows the construction, the circuit symbol and the V–I characteristics of a TRIAC.

A device similar to TRIAC in construction, but without the gate terminal is the silicon bilateral switch (SBS). Its characteristics are symmetrical and it switches ON and breaks down for applied voltage of both polarities.

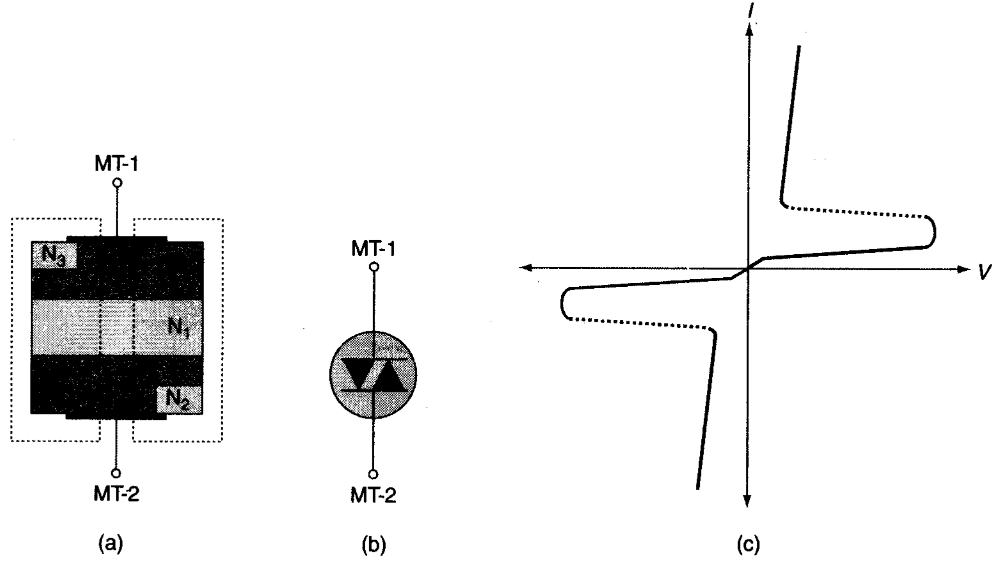


Figure 6.21 | DIAC: (a) Construction; (b) circuit symbol; (c) V–I characteristics.

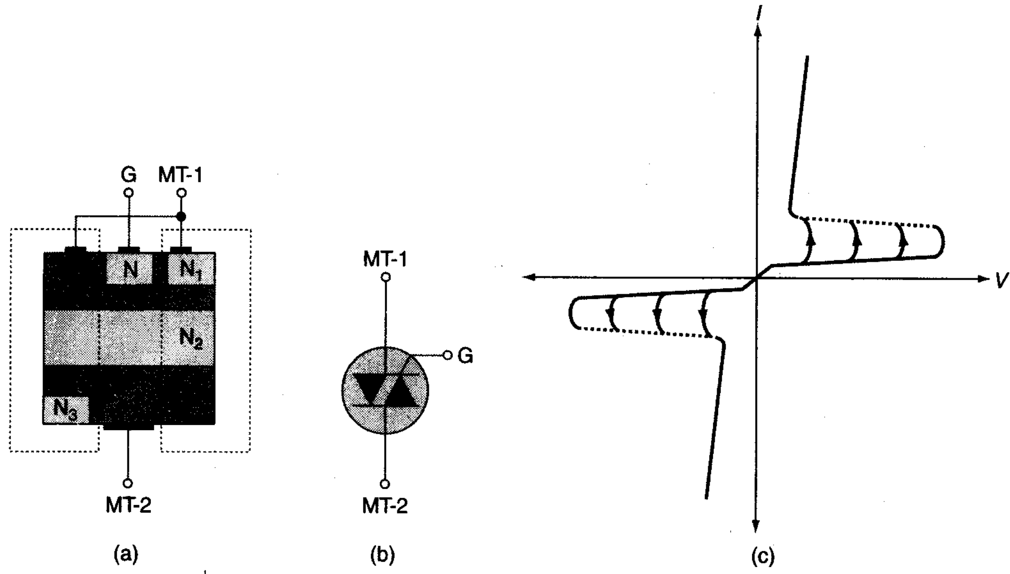


Figure 6.22 | TRIAC: (a) Construction; (b) circuit symbol and (c) V–I characteristics.

6.5 Thyristor Parameters

Major performance specifications of a thyristor include the following:

1. Repetitive peak reverse voltage, V_{RRM}.
2. Non-repetitive peak reverse voltage, V_{RSM}.

3. Repetitive peak OFF-state voltage, V_{DRM}.
4. Break-over voltage, V_{BO}.
5. Critical rate of rise of ON-state current (di/dt).
6. Critical rate of rise of OFF-state voltage (dv/dt).
7. Holding current, I_H.
8. Holding voltage, V_H.
9. Latching current, I_L.
10. Amperes squared seconds (I^2t) rating.

Repetitive Peak Reverse Voltage

Repetitive peak reverse voltage (V_{RRM}) is defined for reverse-blocking mode of thyristors like SCRs for operation in the third quadrant (Figure 6.23). It is the maximum repetitive reverse voltage (anode negative with respect to the cathode) that can be applied to the device safely while still keeping it in the blocked state. The current that flows through the device in this state is referred to as the repetitive peak reverse current (I_{RRM}).

Non-Repetitive Peak Reverse Voltage

Non-repetitive peak reverse voltage (V_{RSM}) as shown in Figure 6.23 is also defined in a similar way. For obvious reasons, this rating is little higher than the one discussed above. If the application is such that the reverse voltage does not appear across the device repetitively, may be because the device is being operated in the forward OFF-state and if it is to be protected against any occasional reverse transients, then V_{RSM} and not V_{RRM} is the rating we should look for. In practice, if we do not allow reverse voltage to exceed V_{RRM}, we are very safe.

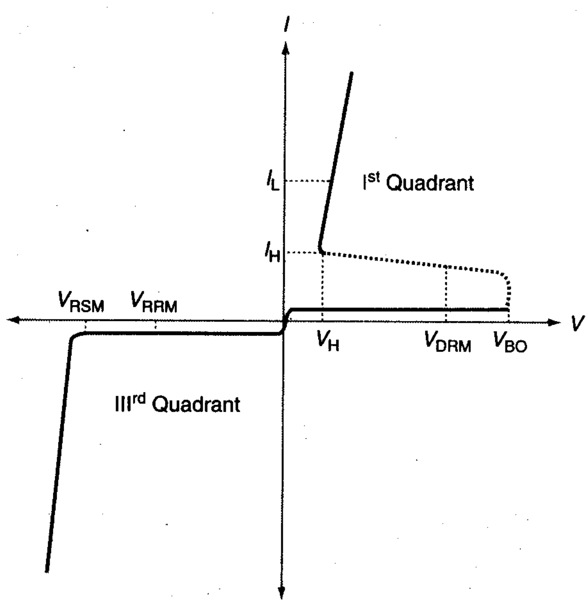


Figure 6.23 | Thyristor parameters.

Repetitive Peak OFF-State Voltage

Repetitive peak OFF-state voltage (V_{DRM}) as shown in Figure 6.23 is the maximum forward OFF-state voltage (anode positive with respect to cathode) that can be allowed to appear across the device when it is being operated in the first quadrant (in the forward-blocking mode). This voltage is usually much less than the actual break-over voltage (V_{BO}) of the device, which is basically a characteristic of the construction of the thyristor. The maximum value of current that can flow in the forward-blocking state is designated as I_{DRM}.

Break-Over Voltage

Break-over voltage (V_{BO}) or peak OFF-state voltage (V_{DM}) is the maximum OFF-state voltage (Figure 6.23). If the applied forward voltage were greater than the break-over voltage, the device is switched to the ON-state even in the absence of any gate signal. The value of V_{BO} does not depend upon the voltage grades of different thyristors in the same family. For instance, SCRs TY 505 F, TY 1005 F, TY 2005F, TY3005 F, TY 4005 F and TY 5005 F, respectively, have V_{DRM} rating of 50, 100, 200, 300, 400 and 500 volts whereas V_{BO} for all these devices belonging to the same class may be larger than the highest available V_{DRM} rating in this class. However, it may be emphasized here that V_{DRM} should not be allowed to exceed in order that the device retains its listed characteristics. The current corresponding to the break-over voltage (V_{BO}) is called break-over current (I_{BO}).

Critical Rate of Rise of ON-State Current

When a thyristor is switched ON, initially, the thyristor can handle a very small current as it is concentrated in a small area of the device pellet. Gradually, the load-current-carrying capability increases to its specified rating. Critical rate-of-rise of ON-state current (di/dt) tells us about the maximum rate of change of ON-state current the device can handle safely. If this rating is exceeded during device switch ON, may be due to a faster switch ON, there could be a development of localized hot spots in the pellet at the time of switch ON and this could result in the device getting damaged. di/dt rating of 100 A/μs is typical.

Critical Rate of Rise of OFF-State Voltage

The critical rate of rise of OFF-state voltage (dv/dt) determines the maximum allowable rate of change of applied forward OFF-state voltage. When applied forward voltage is a time-varying one, a current equal to $C \times dv/dt$ flows through the reverse-biased junction capacitance (C) of the thyristor. This current if more than a certain value can cause premature firing of the thyristor due to decrease in its break-over voltage. Maintaining dv/dt within dv/dt rating of the device ensures that there is no change in the break-over voltage (V_{BO}) of the device. A dv/dt rating of 100 V/μs is quite common.

The dv/dt rating can be enhanced by connecting a low resistance between gate and cathode, thus providing a low resistance shunt path for the changing current mentioned above bypassing gate-cathode junction. Majority of high dv/dt-rating thyristors use what is called a shorted emitter construction which is nothing but an internally created low-value resistance across gate-cathode junction.

Holding Current and Holding Voltage

Holding current (I_H) and *holding voltage* (V_H) are defined when the device is in the ON-state and has to be kept there only. Now if the voltage across the device is decreased so that the current decreases, then at a particular stage, the current is not able to keep the device in the ON-state. So, the device goes to OFF-state. Holding current (Figure 6.23) is minimum ON-state current required to keep the thyristor in the low impedance state once it has been triggered to the ON-state. In order to switch off the thyristor, the anode current must be brought below the holding current value. Voltage corresponding to holding current is termed as holding voltage.

The values of these parameters vary from type to type. Typical value of holding current may lie between several milliamperes to several hundreds of milliamperes. Holding voltage may be as small as 0.5 V for smaller units and as large as 20 V for larger devices. Furthermore, these values are subject to change with temperature.

Latching Current

Latching current (I_L) is little larger than the holding current and ON-state current equal to or more than the latching current ensures that once the device is switched ON, it remains in the ON-state even after the gate signal is removed. Once the ON-state current has exceeded the latching current value after switch ON, the current then has to be brought below the holding current to switch it OFF. To further illustrate the difference, let us assume that an SCR is triggered with a narrow gate-trigger pulse and that the gate pulse has been withdrawn before the anode current of the triggered device could reach the latching current amplitude. In such a case, the ON-state will not sustain and the device will come back to the forward-blocking state immediately after the gate-trigger pulse is withdrawn.

Amperes Squared Seconds (I^2t) Rating

The *amperes squared seconds* (I^2t) rating of a thyristor tells us about the surge current-handling capability of the device for sub-cycle time periods when the device is being used as a rectifier. I^2t rating is usually specified in the data sheet. It can also be calculated from the maximum peak surge current that the device can sustain for a given time period which is usually one full cycle of an applied 50 Hz/60 Hz waveform. I^2t rating of the thyristors can be used to calculate the surge current capability when the thyristor conducts for only a part of the full cycle time period.

6.6 Thyristors as Current-Controllable Devices

Thyristors are negative resistance devices as a part of their V–I characteristics exhibits negative resistance where a reduction in the voltage is accompanied by an increase in current. As an example, Figure 6.24 shows the V–I characteristics of a PNPN diode and existence of negative resistance region.

Thyristors are current-controllable devices because their V–I characteristics can be expressed by a single-valued function of current. That is, for every current value, there is one and only one corresponding voltage value (Figure 6.24). For instance, for current equal to 30 mA and 40 mA, the corresponding voltages are 0.5 V and 0.7 V, respectively. On the other hand, these characteristics are representative of a multivalued function

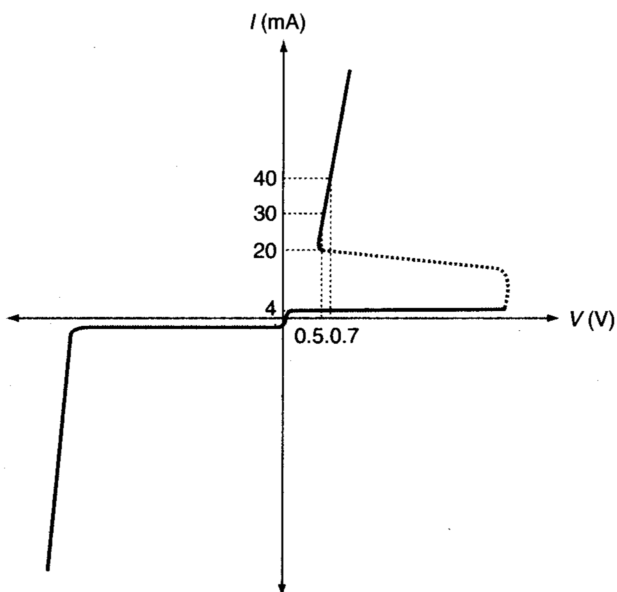


Figure 6.24 | V–I characteristics of PNPN diode – negative resistance region.

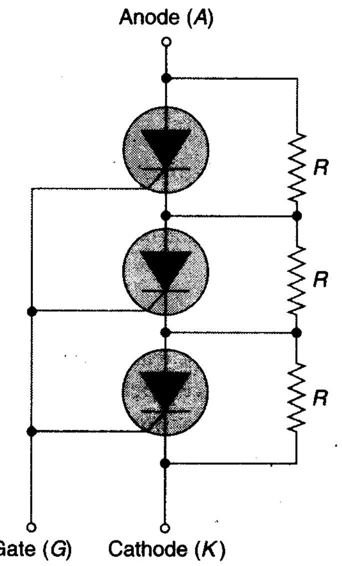


Figure 6.25 | Thyristors in series.

of voltage. That is, for every voltage value, there could be one or more than one corresponding current values. For instance, for a voltage of 0.7 V, the current could be 4 mA or 20 mA or 40 mA. Of course, 20 mA point is in the unstable region and cannot thus sustain. It is because of "single-valued function of current" and "multi-valued function of voltage" nature of the V–I characteristics that thyristors are considered as current-controllable devices. UJTs also belong to the same class.

6.7 Thyristors in Series

Thyristors are connected in series to enhance the voltage rating of the individual devices. For instance, two SCRs each having a repetitive peak OFF-state voltage rating (V_{DRM}) of 1000 V could be connected in series to get an overall V_{DRM} of 2000 V provided that steps are taken to ensure that the applied voltage is equally divided between the individual devices. The device to be connected in series should preferably have closely matched OFF-state characteristics like forward break-over voltage, OFF-state resistance and so on. One way to force an equal division amongst individual devices is to connect identical resistors across each one of the device connected in series (Figure 6.25). The value of R here should be a fraction of the forward OFF-state resistance so that any variation in this parameter from device to device does not affect the voltage division. Capacitive dividers are also used as the resistors dissipate power and reduce the efficiency. In the case of capacitive dividers, a series resistance should be used alongwith each capacitor to damp the current pulses.

6.8 Thyristors in Parallel

Thyristors are connected in parallel to enhance the current capability of the individual devices to be connected in parallel. Care should, however, be taken to ensure that the total ON-state current is equally divided amongst individual devices connected in parallel. To achieve this, the devices should preferably have closely matched forward conduction characteristics like the ON-state dynamic impedance, ON-state voltage and so on. Equal division of current can be forced by connecting small resistors in series with each of the parallel connected thyristors (Figure 6.26). R in this case is much larger than the ON-state dynamic impedance of the individual thyristors.

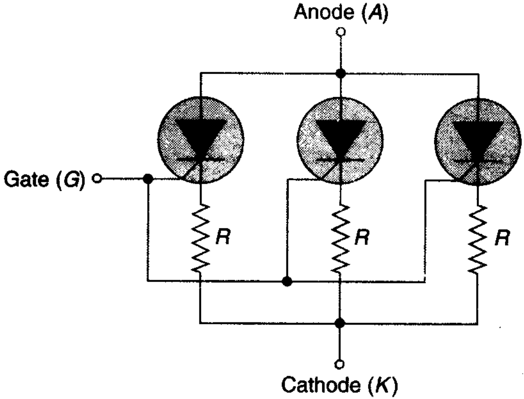


Figure 6.26 | Thyristors in parallel.

6.9 Applications of Thyristors

Some common applications of devices of thyristor family are briefly discussed in the following sub-sections.

SCR as Pulse Generator

Figure 6.27 shows the use of an SCR as a pulse generator. In the normal state, the output voltage would be at ground level as the capacitor C_1 would have been sitting charged to V volts. It may be at mentioned that the break-over voltage of the SCR must be greater than the voltage V. When a triggering pulse is applied at the gate of the SCR, it fires and the capacitor C_1 discharges through ON resistance (r) of the SCR and resistance R_1. It does so with a time constant R_1C_1 if $r < R_1$. The capacitor can discharge only upto a voltage V_H (called holding voltage) as beyond that holding current of the SCR can no longer be supplied and the SCR turns off. When the SCR fires, the voltage across SCR tends to change abruptly to V_H from V changing by $(V-V_H)$. Since, voltage across a capacitor cannot change abruptly, the output voltage (V_o) changes abruptly from 0 to $-(V-V_H)$ and then rises exponentially as C_1 discharges. The output abruptly goes to zero when voltage across C_1 has decayed to V_H which can no longer supply the holding current (I_H) and at that instant $V_o = I_HR_1$. The output pulse-width in this case is about $3R_1C_1$.

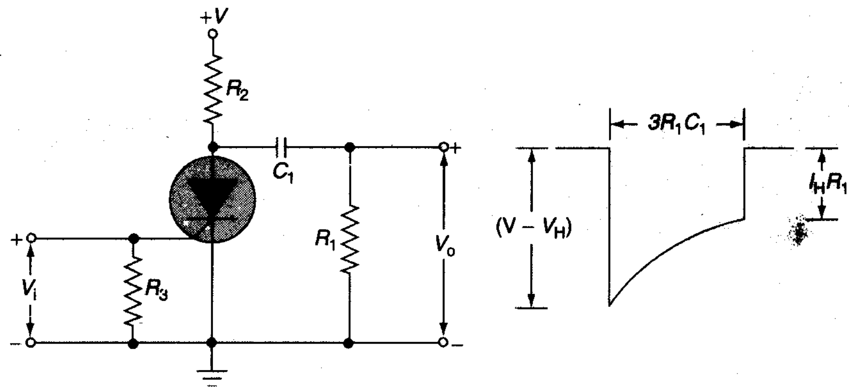


Figure 6.27 | SCR-based pulse generator.

SCR as Bistable Multivibrator

Figure 6.28 shows the basic circuit arrangement of a bistable multivibrator using SCRs. In the circuit arrangement shown, if the supply voltage is less than the break-over voltage of the SCRs, the circuit can be used as a bistable multivibrator. If the supply voltage is greater than the break-over voltage, it becomes an astable multivibrator with the frequency of oscillation determined by R_1, R_2 and C.

In the bistable mode, the circuit functions as follows. Assume that SCR-1 is initially conducting and SCR-2 is in cut-off. Obviously, the output voltage is low (= V_H). Under these conditions, the current flowing through SCR-1 is limited by R_1 only.

R_1 can be chosen in such a way that current through SCR-1 is only slightly greater than the holding current. Now if we apply a positive trigger at the gate of SCR-2, it starts conducting and the anode voltage of SCR-2 drops from V to V_H. This abrupt change is transmitted to the anode of SCR-1 as voltage across C cannot change instantaneously. This negative-going step at SCR-1 anode turns it OFF. Also the current that flows through C as a result of SCR-2 anode going to an almost zero potential has to be supplied through R_1. As mentioned above, R_1 cannot supply both the holding current for SCR-1 as well as current through C. As a result, current through SCR-1 falls below its holding current value and its turn-OFF is ensured. As SCR-1 goes to OFF-state, output goes high (= V). A positive trigger at SCR-1 gate again changes state.

Half-Wave Controlled Rectifier

The basic circuit diagram is shown in Figure 6.29. The point at which the gate-trigger pulse is applied to the SCR gate during the positive half cycle of the AC source is controlled by a suitable circuitry in the box labeled "phase control". During the negative half cycle, SCR remains reverse-biased and there is no current through the load. Thus, input AC power appears across the load only during the conduction period of the SCR. The AC power in the load thus can be controlled by controlling the firing angle of SCR.

Figure 6.30 shows the relevant waveforms. Figure 6.30(a) shows the waveforms appearing across the load and Figure 6.30(b) shows SCR anode waveform. In the half-wave rectifier control of AC power using SCR, the firing angle can be anywhere between 0° and 180°.

Full-Wave Controlled Rectifier

The basic circuit arrangement is shown in Figure 6.31. Typical input and output waveforms are shown in Figure 6.32. Conduction angle is 90°. Diodes D_1 and D_3 conduct during positive half cycles of

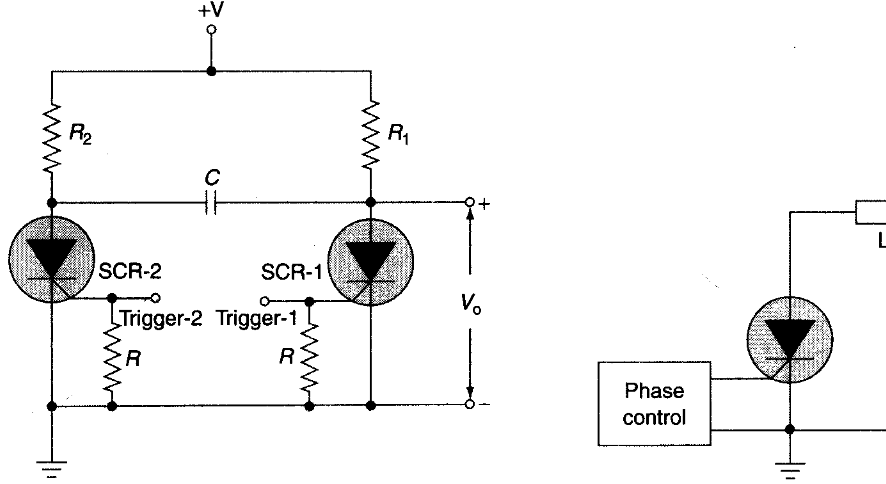


Figure 6.28 SCR-based bistable multivibrator.

Figure 6.29 Half-wave controlled rectifier.

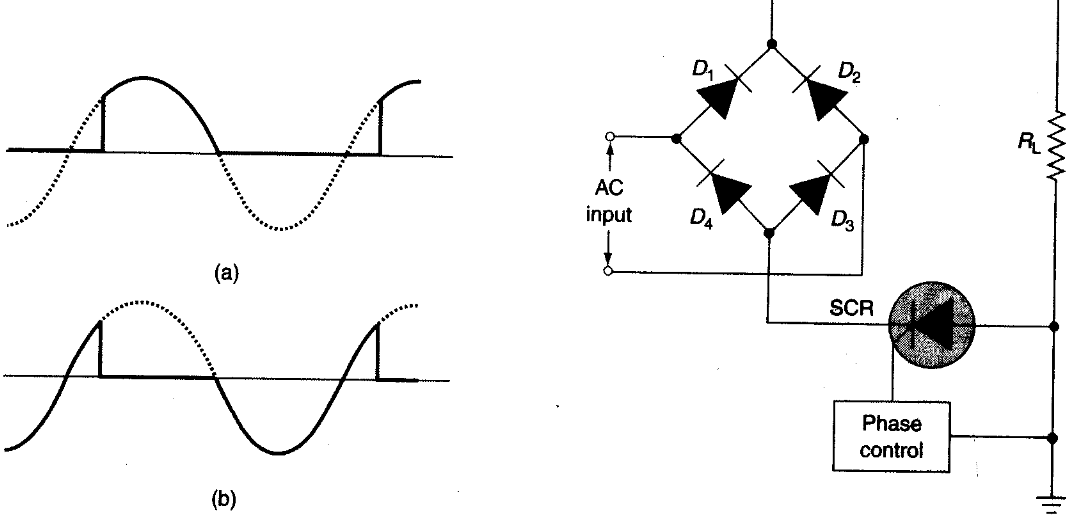


Figure 6.30 | Relevant waveforms in half-wave controlled rectifier.

Figure 6.31 | Full-wave controlled rectifier.

input whereas diodes D_2 and D_4 conduct during negative half cycles of input. The power control is provided by SCR.

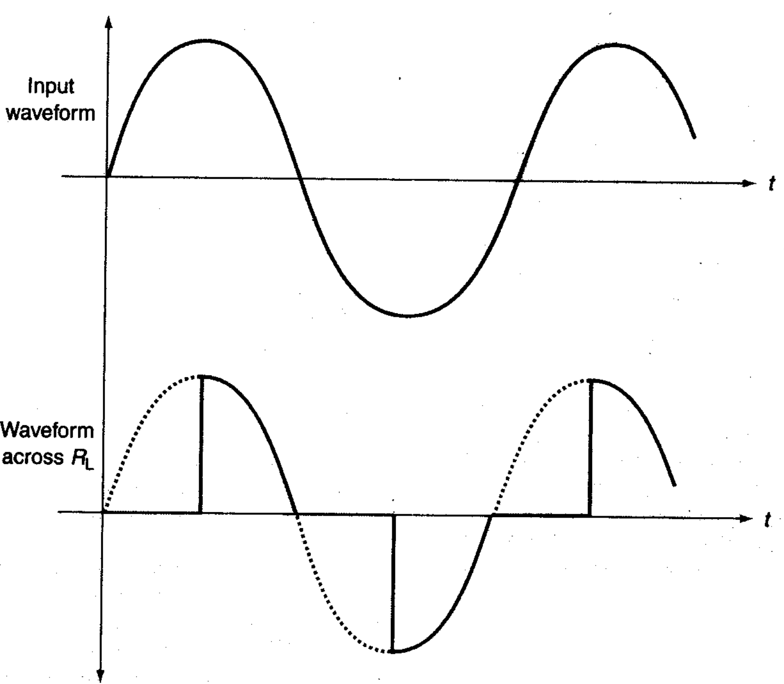


Figure 6.32 | Relevant waveforms in full-wave controlled rectifier.

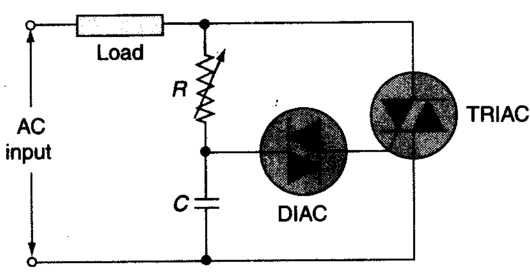


Figure 6.33 | TRIAC-based AC power control.

TRIAC-Based AC Power Control

Figure 6.33 shows basic circuit arrangement. The portion of input AC power that appears across the load is during the time the TRIAC is ON. The idea is similar to the one discussed in the case of an SCR with the TRIAC having an advantage that it can control both positive as well as negative half cycles. In the circuit shown, phase angle is being controlled by a DIAC. During both positive and negative half cycles, the TRIAC conducts as and when the break-over voltage of the DIAC is exceeded.

The TRIAC turns off when the current falls below its holding value. Another trigger during the negative half cycle turns the TRIAC ON again. The period for which the TRIAC conducts during positive and negative half cycles of AC input can be controlled by varying R. By controlling time constant (RC), we can control the time instant at which DIAC would fire which in turn triggers the TRIAC.

SCR-Based Crowbar Protection

An SCR crowbar circuit protects the output voltage of a power supply from becoming excessively high. This is particularly important in the power supplies designed for feeding sensitive loads such as digital integrated circuits. The operational principle of an SCR crowbar can be explained with the help of schematic arrangement of Figure 6.34.

The over-voltage at which crowbar action occurs is given by $V_Z + V_{GT}$. V_Z is obviously selected to be higher than the normal operating voltage of the power supply. The crowbar circuit remains inactive as long as the power supply output voltage is less than $V_Z + V_{GT}$. If the output voltage exceeds $V_Z + V_{GT}$, SCR is triggered. It shorts the load, thus protecting the load from excessive voltage. Crowbar is always used in conjunction with a fuse or some kind of current limiting to protect the power supply.

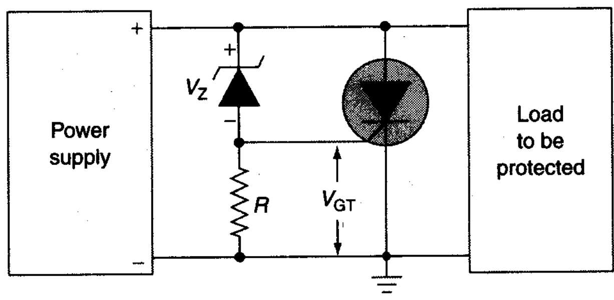


Figure 6.34 | SCR crowbar circuit.

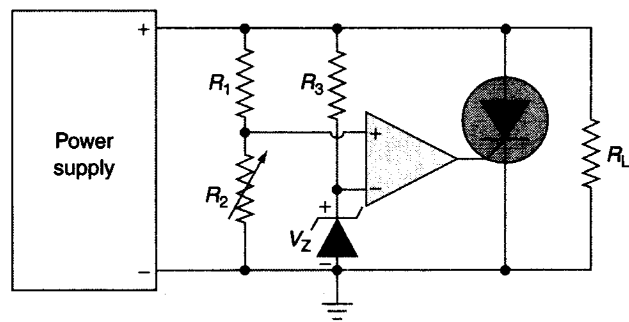


Figure 6.35 | Modified SCR crowbar circuit.

An important aspect of crowbar circuit is its turn-ON time. Since SCRs with turn-ON time as fast as a microsecond are commercially available, it suits the application. In the basic circuit of Figure 6.34, the turn-ON of SCR is dependent on the breakdown of Zener diode. Owing to a slightly curved knee of the Zener diode characteristics at the breakdown point, the device becomes a bit sluggish. The problem can be overcome by adding gain to the trigger circuit of SCR. One such circuit is shown in Figure 6.35. The circuit is self-explanatory.

Crowbar action occurs at an output voltage given by

$$V_O \times \frac{R_2}{R_1 + R_2} = V_Z \tag{6.10}$$

$$V_O = V_Z \times \left(1 + \frac{R_1}{R_2}\right) \tag{6.11}$$

Crowbar circuits are now available in IC form for a range of standard operating voltages. These ICs just need to be connected across the load. The IC crowbar has a built-in Zener diode, some kind of gain circuit and SCR. SK 9345 series of IC crowbars offer protection to +5 V (SK 9345), +12 V (SK 9346) and +15 V (SK 9347) power supplies.

EXAMPLE 6.5 *Refer to the SCR-based half-wave power control circuit of Figure 6.36. The 230 V AC source of supply feeds a 100 Ω load through a controlled rectifier. If the trigger circuit of the SCR was so adjusted as to start conduction at 30° after the start of each cycle, determine the total power delivered to the load by the AC supply. Assume holding voltage of the SCR to be zero.*

Solution

1. The instantaneous value of the power drawn from the AC supply is the product of the instantaneous values of line current and line voltage. The average value of this product will be the power delivered by the AC supply.
2. The SCR conducts only for a period from 30° ($\pi/6$ rad) to 180° (π rad) during each cycle. For rest of the period, the SCR remains in the cut-off state.
3. Therefore, the current flows through the load only for a period from 30° ($\pi/6$ rad) to 180° (π rad).
4. The expression for instantaneous value of line current is given by

$$(230 \times \sqrt{2}/100) \sin \alpha = 3.252 \sin \alpha$$

5. The expression for instantaneous value of line voltage is given by

$$(230 \times \sqrt{2}) \sin \alpha = 325.2 \sin \alpha$$

6. The expression for power therefore is given by

$$P = \frac{1}{2\pi} \times \int_{\pi/6}^{\pi} (3.252\sin\alpha) \times (325.2\sin\alpha)d\alpha = \frac{1}{2\pi} \times \int_{\pi/6}^{\pi} 1057.6\sin^2\alpha d\alpha$$

7. After integration operation, the above expression reduces to

$$P = \frac{1}{2\pi} \times \left|528.8\alpha - (528.8/2)\sin 2\alpha\right|_{\pi/6}^{\pi}$$

8. This simplifies to $P = 256.78$ W.

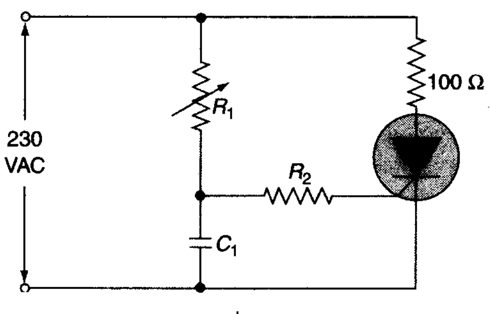


Figure 6.36 | Example 6.5.

EXAMPLE 6.6 *Refer to the SCR crowbar circuit of Figure 6.37. Determine the required breakdown voltage of the Zener diode if the load voltage could at the most be allowed to increase to 10 V. Take V_{GT} of SCR to be equal to 0.8 V.*

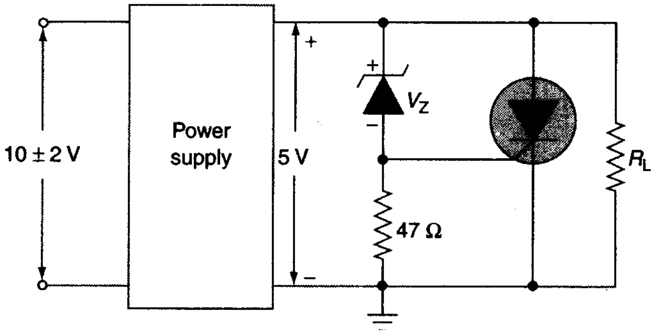


Figure 6.37 | Example 6.6.

Solution

1. In the present case, $V_Z + V_{GT} = 10$ V.
2. This gives $V_Z = 10 - V_{GT} = 10 - 0.8 = 9.2$ V.

6.10 Gate Turn-OFF Thyristors

A conventional thyristor as described in the preceding sections is a solid-state semiconductor device with at least four layers of alternating P and N types of semiconductor material. These devices can be with or without the gate control terminal and act like a latching-type switch. These devices continue to stay in the conducting state once they are appropriately triggered as long as the voltage across the device is not reduced to zero or reversed or the forward current brought below a certain threshold value called the holding current.

A gate turn-OFF thyristor (GTO), on the other hand, is a special type of thyristor, which can be switched to the ON and OFF states by applying appropriate trigger pulses to the gate terminal. The GTO can be turned ON by a positive current pulse applied between gate and cathode terminals. The turn-ON phenomenon in a GTO is not as reliable as it is in the case of a conventional thyristor. A small magnitude of positive gate current therefore must be maintained even after turn-ON to improve reliability.

The turn-OFF of the GTO is accomplished by applying a suitable negative voltage pulse. Application of negative voltage initiates a reduction in the forward current by about 20–30%. This reduction in forward current induces a cathode-to-gate voltage which further reduces the forward current. The process ultimately culminates in the device transitioning to the blocking state.

As compared to conventional thyristors, GTO thyristors have relatively higher ON-state voltage drop, longer turn-ON and turn-OFF times and also require higher turn-ON gate current.

GTO thyristors are available without or with reverse-blocking capability. The former are known as asymmetrical GTO thyristors, abbreviated as A-GTO. The GTO thyristors with reverse-blocking capability are known as symmetrical GTO thyristors, abbreviated as S-GTO. The major application areas of GTO thyristors include their use in variable speed motor drives, high power inverters and traction.

6.11 Programmable Unijunction Transistor

The conventional unijunction transistor is essentially a lightly doped bar of N-type semiconductor material with heavily doped P-type diffusion region somewhere along the length of the bar. The diffusion point is usually closer to one of the ends of the N-type bar.

Programmable unijunction transistor (PUT) behaves more or less like a UJT and has similar applications. A PUT is designed to enable the engineer to program UJT parameters, which include inter-base resistance (R_{BB}), intrinsic stand-off ratio (η), peak current (I_P) and valley current (I_V). Programming is possible with the help of two external resistors. Figure 6.38(a) shows the circuit symbol and Figure 6.38(b) the constructional features of a PUT device. R_1 and R_2 are programming resistors. R_{BB} and η in the case of PUT are given by Eqs. (6.12) and (6.13), respectively. The peak current and valley current depend upon the equivalent resistance R_G of the gate control circuit. R_G is given by Eq. (6.14).

$$R_{BB} = R_1 + R_2 \quad (6.12)$$

$$\eta = R_1/(R_1 + R_2) \quad (6.13)$$

$$R_G = R_1 \times R_2/(R_1 + R_2) \quad (6.14)$$

As is obvious from Figure 6.38(b), the name PUT is a misnomer. PUT is a four-layer device like a thyristor with contacts, namely, anode (A) and cathode (K) made to the two extreme layers and a control contact called gate (G) made to one of the inner layers. In this case, the inner layer chosen is the one closer to the

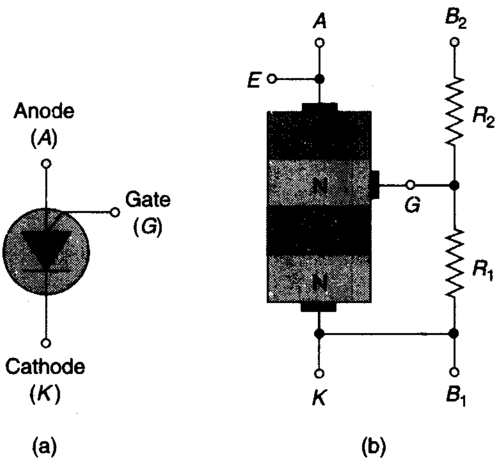


Figure 6.38 | Programmable unijunction transistor: (a) Circuit symbol; (b) construction.

anode contact. The device is so called because it can perform functions similar to that of a UJT. Note that a PUT device is directly interchangeable with a UJT device.

Figure 6.39 shows the V–I characteristics of a PUT device. The voltage V_S appearing at the control terminal is given by

$$V_S = V_B \times [R_1/(R_1 + R_2)] \tag{6.15}$$

where V_B is the DC voltage applied between B_2 and B_1 terminals.

As anode to cathode voltage exceeds V_S by one diode voltage drop, the device goes to conduction. We can notice the similarity in the V–I characteristics of a PUT and a UJT device. 2N 6027 and 2N 6028 are commonly used PUTs. Like UJT devices, the most common application of PUT devices also is in triggering of thyristors. Figure 6.40 shows one such circuit, which is self-explanatory.

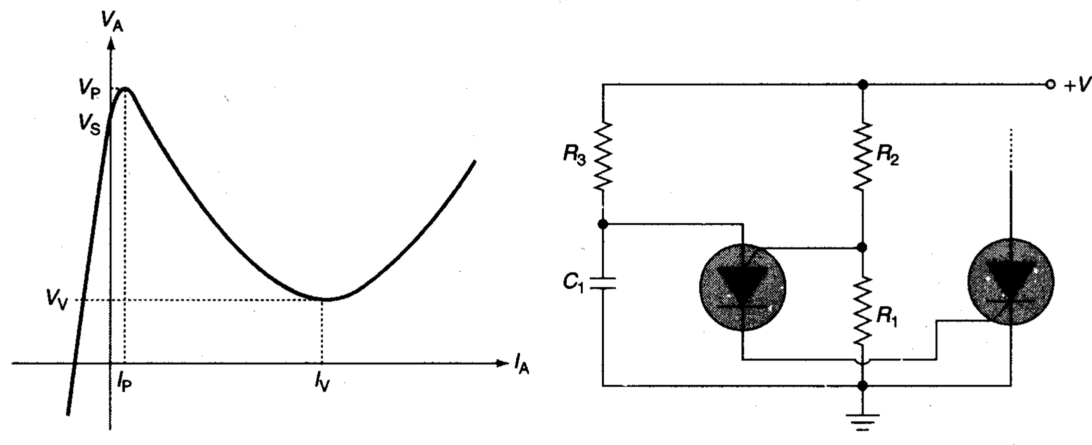


Figure 6.39 | V–I characteristics of PUT.

Figure 6.40 | Thyristor triggering with a PUT device.

KEY TERMS

Amperes squared seconds rating
Asymmetrical gate turn-OFF thyristor
Break-over voltage
Critical rate of rise of OFF-state voltage
Critical rate-of-rise of ON-state current
DIAC
Gate turn-OFF thyristor
Holding current
Holding voltage
Intrinsic stand-off ratio
Latching current
Non-repetitive peak reverse voltage
Peak OFF-state voltage
PNPN diode
Programmable unijunction transistor
Rate effect
Repetitive peak OFF-state voltage
Repetitive peak reverse voltage
Silicon-controlled rectifier
Symmetrical gate turn-OFF thyristor
Unijunction transistor
TRIAC

OBJECTIVE-TYPE EXERCISES

Multiple-Choice Questions

1. SCRs are connected in series to enhance
   a. their overall d*v*/d*t* rating.
   b. the overall voltage rating.
   c. their current-handing capability.
   d. none of these.
2. While connecting SCRs in series, the individual SCRs chosen for the purpose should have closely matched
   a. d*i*/d*t* rating.
   b. reverse-biased characteristics.
   c. forward- and reverse-blocking characteristics.
   d. forward ON-state characteristics.
3. SCRs are connected in parallel to enhance
   a. voltage-handing capability.
   b. current-handing capability.
   c. d*i*/d*t* rating.
   d. none of these.
4. While connecting SCRs in parallel, the SCRs to be connected in parallel should have closely matched
   a. forward ON-state characteristics.
   b. forward and reverse OFF-state characteristics.
   c. forward OFF-state and ON-state characteristics.
   d. SCRs cannot be connected in parallel.
5. A UJT relaxation oscillator circuit produces a sawtooth like waveform
   a. at B_1 terminal.
   b. at B_2 terminal.
   c. across the capacitor.
   d. none of these.
6. V–I characteristics of a UJT can be expressed by
   a. a single-valued function of voltage.
   b. a multi-valued function of current.
   c. a single-valued function of current.
   d. none of these.
7. Which of the following device type numbers is not a thyristor?
   a. 2N2646
   b. OE 104
   c. TY 1005 F
   d. OE 106
8. Pick the odd one out.
   a. Tunnel diode
   b. UJT
   c. SCR
   d. TRIAC
9. When we want to know the sub-cycle surge current capability of a thyristor, we should look for
   a. d*i*/d*t* rating.
   b. surge current rating, I_{FSM}.
   c. I^2t rating.
   d. none of these.

10. In half-wave SCR power control circuit, if the firing angle is 30°, then for one complete cycle of operation, the load gets power for
    a. 60°
    b. 150°
    c. 330°
    d. 30°
11. The construction of a programmable unijunction transistor (PUT) is
    a. similar to that of a conventional unijunction transistor except for the fact that both resistors forming the inter-base resistance R_{BB} are variable.
    b. similar to that of a four-layer PNPN diode.
    c. different from the conventional unijunction transistor in the sense that in the case of a PUT, the silicon bar is heavily doped and the P-type emitter is lightly doped.
    d. different from the conventional unijunction transistor in the sense that a PUT is made from germanium and not silicon.
12. Which of the following thyristors does not have a control terminal?
    a. DIAC
    b. TRIAC
    c. SCR
    d. GTO thyristor
13. While switching an SCR from the forward-blocking state to the ON-state by applying a gate-trigger pulse, it is important for a successful switch on that the gate-trigger pulse is present till one of the following parameters is exceeded.
    a. Holding current
    b. Latching current
    c. Holding voltage
    d. di/dt rating
14. Which of the following parameters is programmable in a programmable unijunction transistor?
    a. Intrinsic stand-off ratio
    b. Inter-base resistance R_{BB}
    c. Peak and valley currents
    d. All the above
15. Once an SCR has been switched to the ON-state, the minimum value of the anode current required to keep the device in the ON-state is called
    a. latching current.
    b. trigger current.
    c. holding current.
    d. break-over current.

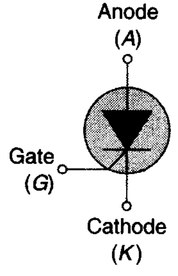
Match the Following

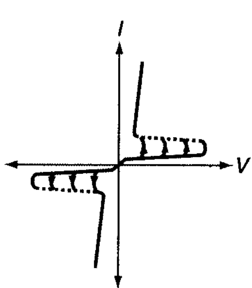
Column 2 of Table 6.1 lists some of the devices belonging to family of UJTs and thyristors from S. No. 1 to 6. Their circuit symbols and the V–I characteristics are given in a haphazard manner in columns 3 and 4 respectively. For each of the listed devices in column 2, identify the corresponding circuit symbol and the V–I characteristics. For example, if you feel that the device listed at S. No. 1 has its circuit symbol and its V–I characteristics, respectively, listed at S. No. 3 and 6, then your answer for this part will be (1–3–6).

Table 6.1

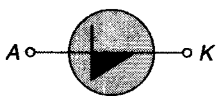
S. No.	Device type	Circuit symbol	V–I characteristics
1.	Silicon-controlled rectifier (SCR)	B_2, E, B_1	V_A, V_S, I_A

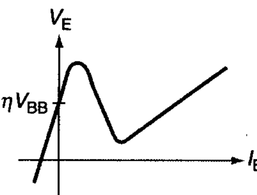
2. Unijunction transistor (UJT)



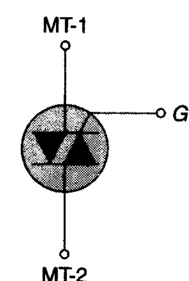


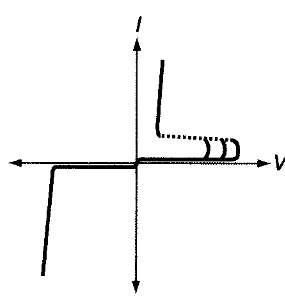
3. Programmable unijunction transistor (PUT)



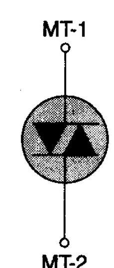


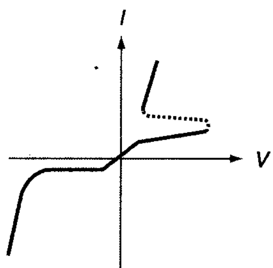
4. DIAC



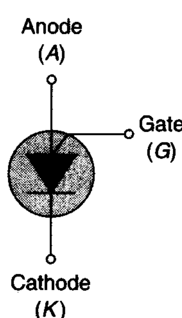


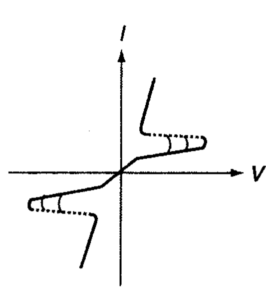
5. TRIAC





6. Silicon-controlled switch (SCS)





REVIEW QUESTIONS

1. What is a unijunction transistor (UJT)? With the help of relevant schematic diagram, briefly describe the operational principle of a UJT with particular reference to its V–I characteristics.

2. Why is UJT referred to as a current-controllable device and not a voltage-controllable device? Draw the basic circuit diagram of a UJT-based relaxation oscillator circuit and derive an expression for its frequency of operation.

3. What is a programmable unijunction transistor (PUT) and how does it differ from a conventional unijunction transistor? What UJT parameters are usually programmable in a PUT?

4. Comment on the following statements.
   a. Programmable unijunction transistor is a close cousin of a thyristor.
   b. It is possible to turn some thyristors off by applying an appropriate signal to the gate.
   c. V–I characteristics of thyristors can be represented by single-valued function of current and multi-valued function of voltage.

5. What is a PNPN diode? Briefly describe the breakdown mechanism in a PNPN diode.

6. How does a silicon-controlled rectifier differ from a PNPN diode? With the help of V–I characteristics, briefly describe the control action of the gate in terms of change in the V–I characteristics as a function of gate current.

7. What do you understand by rate effect in thyristors? How does this lead to premature firing of the device?

8. Define and briefly describe the significance of following electrical parameters of thyristors.
   a. Holding current
   b. Latching current
   c. Critical rate of rise of OFF-state voltage
   d. Critical rate of rise of ON-state current

9. What are gate turn-OFF (GTO) thyristors? Differentiate between asymmetric and symmetric GTO thyristors.

10. With the help of basic circuit diagrams, briefly describe the operation of the following application circuits.
    a. Half-wave AC power control using an SCR
    b. SCR-based crowbar circuit
    c. SCR triggering using a programmable unijunction transistor

PROBLEMS

1. Refer to the UJT-based relaxation oscillator circuit of Figure 6.41 and the associated sawtooth waveform observed across the capacitor. Determine the peak value (V_P) of the sawtooth voltage across the capacitor given that the intrinsic stand-off ratio η of the UJT used in the circuit is 0.4. Assume the forward-biased diode voltage drop of 0.65 V.

2. Refer to the PNPN diode circuit of Figure 6.42. The PNPN diode used in the circuit has a break-over voltage of 12 V and holding and latching current specifications of 5 mA and 10 mA, respectively. Determine the status of LED, whether it is ON or OFF, for (a) $R = 1$ kΩ and (b) $R = 10$ kΩ. Assume the forward-biased drop across PNPN diode and LED to be 1.5 V each.